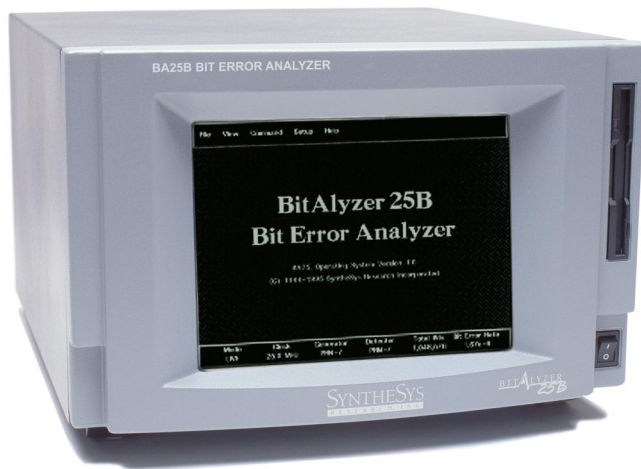


BitAlyzer25B Bit Error Analyzer



FEATURES

- 25 Mbit/sec bit error rate analysis
- BitAlyzer error location analysis
- Complete data generator, analyzer and clock source
- Live or off-line error analysis

The BitAlyzer25B is an error analysis system that provides multiple perspectives of errors in your digital channel. It is composed of a pseudo-random, or 16-bit fixed data pattern generator that is tightly coupled with a precise error detection module. Errors are detected by sending a controlled data pattern into the channel under test and then performing a bit-by-bit comparison. Where a bit error

rate simply tells the ratio of errored data bits to the total number of bits transmitted, the BitAlyzer25B draws on its patented real-time capability to log and analyze the exact bit position of every error in a data stream. On the basis of this error position information, the relationship of errors to their neighbors as well as error correlations can be determined.

BENEFITS

- Advanced analysis for low data rate requirements
- Quickly differentiate types of errors
- Optimizes lab and rack space
- Archive tests to hard disk or floppy disk for later analysis



The touch screen enables operation to be performed via easy-to-use pull-down menus.



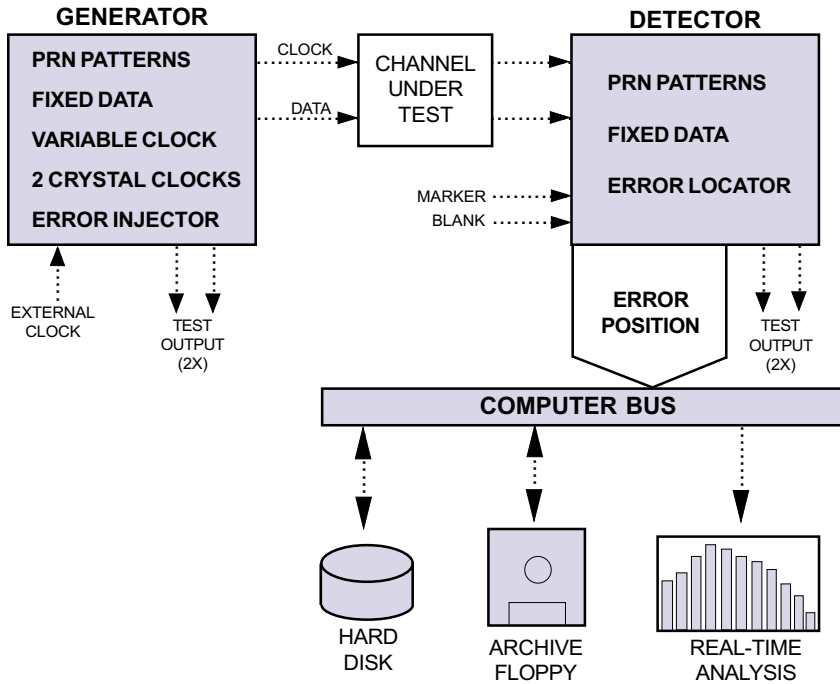
Hardcopy results are available from the built-in parallel printer port.

BitAlyzer[®]25B

SYNTHESYS
RESEARCH, INC.

www.synthesysresearch.com
650 364-1853

SYSTEM BLOCK DIAGRAM



INTERFACING

The BitAlyzer25B connects to your channel via TTL or Differential TTL serial clock and data interfaces. The unit contains a crystal and a voltage-controlled-oscillator clock source, or it can be externally clocked. The unit then transmits one of five pseudo-random patterns or a 16-bit fixed pattern through the channel under test. The detecting circuits are connected to the receiving end of the channel via TTL or Differential TTL

serial clock and data interfaces. The detector can continuously search the incoming stream for the data pattern type; once a pattern is recognized, detailed error analysis can begin.

Other hardware signals that are provided for more sophisticated applications include:

Blank — When this signal is high, detector input is blanked, and error analysis is not performed. Optionally, upon the trailing edge of blank, data resynchronization can be requested.

Marker — Error analysis is tagged when this pulse is received so that correlation between errors and external hardware signals can be analyzed.

Test Outputs — Four test output signals can be assigned to various internal signals, including Error Event, Serial Clock, Blank, Marker, Retrigger, and Serial Data.

ERROR MEASUREMENTS

During error analysis, the BitAlyzer25B can store the errors it locates on its internal hard disk drive. This feature enables live or off-line error measurements. In satellite applications, for instance, access to the channel for testing may be restricted. Using the BitAlyzer25B, only a short amount of downtime is required to acquire error information. Later, the error information can be analyzed to diagnose the problem.

GRAPHICAL ANALYSIS

The BitAlyzer25B analyzes errors to see if they correlate to the type of data pattern in use, to external marker input signals, or to any repetition count that may be a characteristic of the channel being tested. Error Free Interval Histograms can identify non-random sources of error. Errors in Block Histograms can identify error correction strength requirements. Burst Length Histograms can identify error correction interleaving depth requirements.

EXAMPLE ANALYSIS

Basic BER			
	Total	Rate	
Errors	75,140	2.68E-6	
Burst Errors	31,759	1.13E-6	
Non-Burst Errors	43,381	1.55E-6	
Burst Events	1,252	4.47E-8	
Lost Bits	0	0.00%	
Bits	28,032,399,008		
Marker Events	0		
Pattern Events	0		
Resync Events	0		
Squelch Events	0		
Elapsed Block(s)	1,121		
Errored Block(s)	1,121		

Clock: 25.00 MHz Detector: PFM-7 Generator: PFM-7 Integration: 100,000,000 Mode: STOP Progress: IDLE

Basic BER

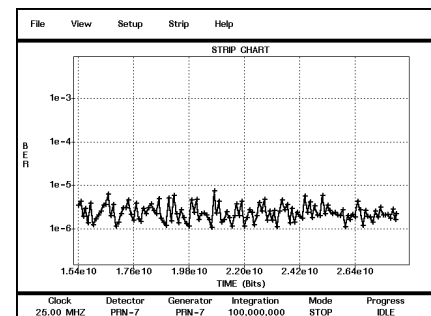
Real-time statistics including errors and bit error rate. Also separates errors into burst and non-burst categories as specified by the user.

CCITT G.821	
Total Test Seconds	438,006
Severely Errored Seconds	64
Number Of Breaks	0
Seconds Of Break	0
Available Seconds	438,006
Available Error Free Seconds	422,824
Available Errored Seconds	15,182
Available Ok Seconds	16,118
Available Seconds Percent	100.00%
Available Ok Seconds Percent	3.45%
Available BER	2.68E-6
Link Status	DISABLED

Clock: 25.00 MHz Detector: PFM-7 Generator: PFM-7 Integration: 100,000,000 Mode: STOP Progress: IDLE

CCITT G.821

Common communications statistics that display link availability per CCITT Recommendation G.821.



BER Strip Chart

Bit, burst, and non-burst error rates are posted at user-selectable integration periods.

ADVANCED COMPUTER CONTROL

The BitAlyzer25B contains a high-speed microprocessor to control a fast touchscreen graphical user interface (GUI). It also provides graphics and text printing. A remote control option is available to control the BitAlyzer25B over an RS-232 or IEEE-488 physical link using simple protocols. Screen printing may also be done to .PCX files, and many analysis features produce comma-separated text files that can be transferred via floppy disk to PC workstations. This data is easily imported into spreadsheet and word processing programs for easy presentation.

CUSTOM CONFIGURATIONS

Individual analysis features have parameters that define how analysis is performed. Examples include mechanisms for defining what a burst error is in the context of the channel under test and mechanisms for defining the integration period over which the bit error rate should be calculated. Each of these parameters is completely under the user's control. Furthermore, once parameters are established, they can be saved in configuration files that completely define an application. These files can be restored in seconds to convert the BitAlyzer25B for use from one application to another.

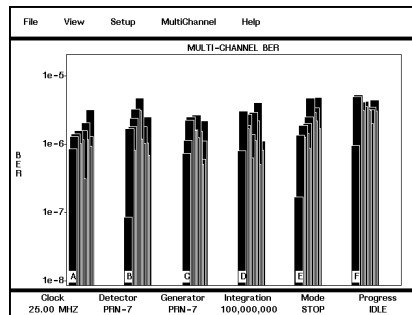
With its lower data rates and serial interface, the BitAlyzer25B is specifi-

cally designed for use in wireless communications, satellite communications, telecommunications, telemetry, read-write channel development, and error correction application areas in the digital tape recording, hard disk, and telecommunications fields.

UNIQUE OPTIONS

Multi-Channel BER Analysis Option

A single communications channel is often actually the result of multiplexing many sub-channels into a single stream. The BitAlyzer25B multi-channel BER analysis option de-multiplexes the errors from the combined stream and attributes them to their source channel. To do this, the number of channels (maximum 32) is specified, along with the number of bits per interleaved block. Then the marker input signal is used to identify the first bit of the first channel. A multi-channel BER analysis display appears as a bar chart over time, on which recent BER postings are drawn in the foreground



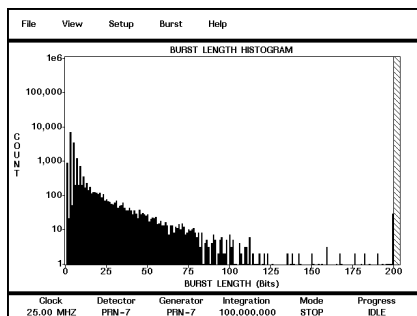
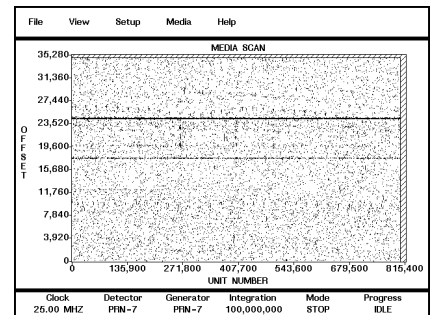
and up to 16 historical values are drawn, fading into the background.

ECC Emulation Option

The Error Correction Emulation option enables ECC system designers to specify certain ECC geometries, interleaving techniques, and correction strengths, and to then perform error analysis on a raw channel as if it employed the specified ECC techniques.

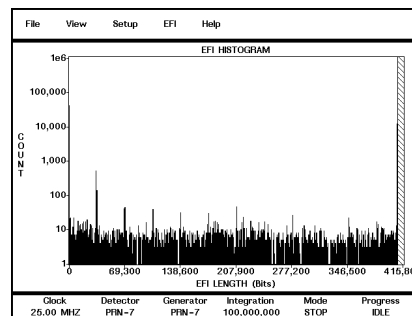
Media Scan, 2-D Error Map Option

For communications systems that have repeating and fixed block sizes, the 2-Dimensional Error Mapping analysis option provides the capability to view the errors from a channel in a rectangular error map. For instance, once a specific quantity of bits is determined to be frame size, and a marker input signal is provided to refer to the beginning of a frame, the BitAlyzer25B draws an X-Y map on which the X-axis represents the frame number and the Y-axis represents the bit position within the frame.



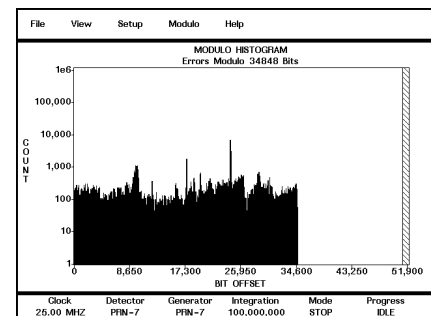
Burst Length Histogram

Probabilities of burst lengths can be used to determine interleaving depth.



EFI Histogram

Histogram of error free distances shows systematic sources of error. Random error free distances would be a "flat" histogram.



Modulo Pattern Histogram

Histogram of errors correlated to a pseudo-random data pattern shows channel sensitivity to portions of the pattern.

SPECIFICATIONS
Data Generator

Data Rate	500 bit/sec to 25 Mbit/sec		
Data Format	True or inverted, serial		
Data Sequences	Pseudo-random sequences:		
	$x^7 + x + 1$ (127 bits)	$x^{11} + x^2 + 1$ (2,047 bits)	
	$x^{15} + x + 1$ (32,767 bits)	$x^{20} + x^5 + 1$ (1,048,575 bits)	
	$x^{23} + x^5 + 1$ (8,388,607 bits)	16-bit user-programmable sequence	
Clock, Data, Blank, Marker	TTL or Differential TTL (family selectable)		

Measurements & Analysis

Direct Measurements	Input Frequency, Input Pattern Type, Output Frequency, Bit Count, Error Count, Bit Error Rate, Burst Error Count, Burst Error Rate, Non-Burst Error Count, Non-Burst Error Rate, Marker Count, CCITT G.821
Accumulate	Bit, Burst, Block and Total Errors, User Bits and Burst Events
Strip Chart	Bit, Burst and Total Error Rates, Marker and Blank Events
Histograms	Burst Length, Error Free Interval, Interval Between Bursts, Errors per User-Defined Block, Modulo- <i>n</i> /Marker (maximum <i>n</i> = 4,294,967,000), Modulo Pattern, Modulo Block
2-D "Media Scan" Error Mapping	Based on Modulo- <i>n</i> or Modulo-Marker (optional)
Error Correction Emulation	2-D Interleave (optional); 1-D Block Code (e.g., Reed-Solomon type); 2-D Block Code; 2-D Block Code with 3-D Interleave
Multi-Channel BER	Bar Chart of up to 32 de-multiplexed channels
Frequency Measurement	Generator: Crystal 1, Crystal 2, Variable, User Clock Input Detector: Clock, Marker, Blank

Data Detector

Error Event Storage:	
Maximum Event Rate	4,000 events/sec (basic live mode); 4,000 events/sec (record mode)

Mainframe

CPU	80486DX-33
Display	640 x 480 LCD B&W VGA flat panel display
Touchscreen	Analog resistive
Random Access Memory	8 MBytes
Disk Storage	200 MByte hard disk (minimum)
Floppy Diskette	1.44 MByte 3.5" MS-DOS compatible

Remote Control (Optional)

Interface	IEEE-488 or RS-232-C
-----------------	----------------------

ORDERING INFORMATION

BA25B	BitAlyzer25B Error Analyzer
BA2ECC	Error Correction Coding Emulation
BA2MEDIA	2D Error Mapping
BA2MULTI	Multi-Channel BER Analysis
BA2IEEE	IEEE-488 Remote Control
BA2SASW	BitAlyzer25B Stand-alone Software
BA23YR	Two Years Added to Standard One-Year Warranty

WARRANTY

All equipment is fully warranted for one year. This includes hardware repair or replacement, at SyntheSys Research's discretion, and software updates. Necessary repairs are performed at the Menlo Park, California factory.

THE COMPANY

Founded in 1989, SyntheSys Research, Inc. is a manufacturer of test instruments for analyzing a variety of digital communications channels. From fiber optics to satellites, hard disks to laser communications, and HDTV to digital television, the company has pioneered innovative techniques into award-winning, user-friendly instruments. SyntheSys Research is driven by the goal of creating quality products needed by industry professionals.



3475-D Edison Way
Menlo Park, CA 94025 U.S.A.
Voice 650 364-1853
Fax 650 364-5716
info@synthesysresearch.com
www.synthesysresearch.com