

# BitAlyzer®1000 Bit Error Analyzer



The BitAlyzer1000 bit error rate analyzer provides many perspectives of your digital channel's error performance. Ideal for applications in recording systems' read/write channels, communications systems, and telemetry links, the BitAlyzer1000 provides the quality analysis needed for design debug, certification, and monitoring of digital signals. It comes complete with an active matrix color touchscreen display, printer port support, floppy interface, and IEEE-488 remote control interface.

The BA1000 comprises a pseudo-random (or optional user-defined) pattern generator, an internal clock synthesizer, and a patented error location and logging receiver. BitAlyzer's unique error location analysis studies the exact bit location of errors in the data stream to show error relationships and correlations.

Error location analysis includes separating user-defined bit errors from burst errors and showing each error measurement separately, allowing the

display of the distribution of error occurrences by their length. Intervals between errors are monitored to show if certain intervals may occur more frequently than others—indicating a systematic error. Exact bit error locations are used to prepare a histogram of the number of occurrences of errors at individual positions within repeating user-defined periods. These periods can be defined by an externally applied Marker input, allowing for perfect correlation to application-dependent sectoring or packetization. Errors are further analyzed on the boundaries of user-defined periods, allowing traditional CCITT G.821 and G.826 measurements as well as a histogram of the number of occurrences of periods with varying numbers of errors in them.

Other forms of BitAlyzer error location analysis include directly displaying the autocorrelation of error position, which clearly identifies systematic error phenomena where one error will predict the presence of a future error.

## FEATURES

- 1000 Mbit/sec Bit Error Rate Analysis
- Serial, 8-bit and 16-bit Data Interfaces
- BitAlyzer Error Location Analysis
- Complete Data Generator, Analyzer, and Clock Source
- Real-Time Error Location Logging of 2.5 Billion Errors
- Live or Offline Error Analysis
- 4-Mbit User Pattern Memory

## BENEFITS

- Serial and Parallel data interfaces
- Bit and burst errors measured separately
- Real-time histograms describe error characteristics of system under test
- Measurement session can be logged for offline analysis
- Remote control of all functions
- Plug-compatible with BA622 BitAlyzer

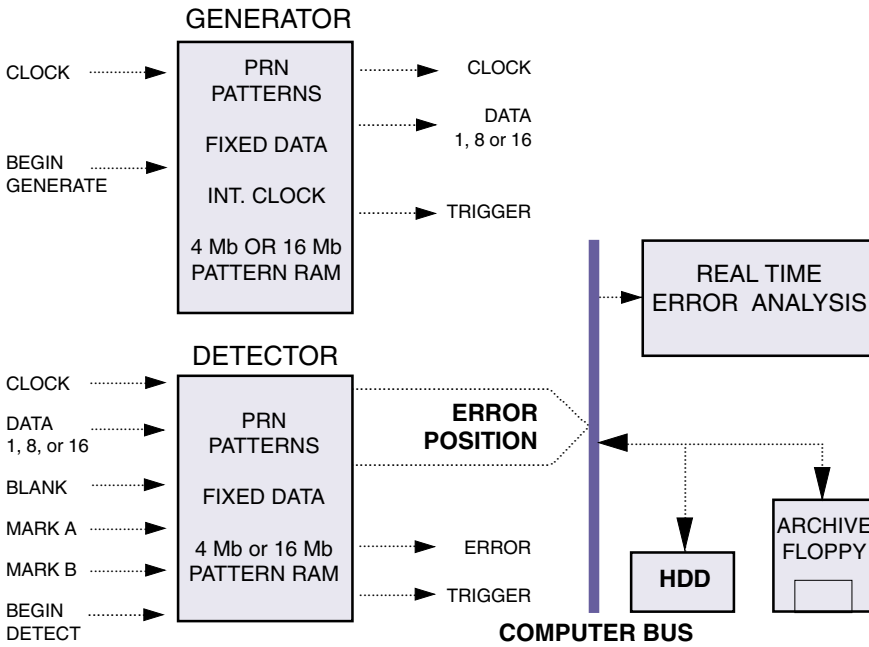
BitAlyzer®1000

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# BitAlyzer<sup>®</sup>1000

## SYSTEM BLOCK DIAGRAM



## PATTERN GENERATOR

The BitAlyzer1000's internal data generator can generate serial, 8-bit, or 16-bit parallel data streams. The data streams can be one of four pseudo-random data sequences, a user-defined 4 Mbit sequence, or an optional 16-Mbit

sequence. The pseudo-random data sequences vary in repeating duration from 127 bits to 8.3 Mbits. The data generation rate is controlled by either an optional clock synthesizer or an externally applied clock input.

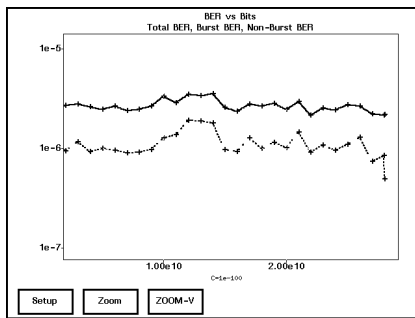
## PATTERN DETECTOR

In the BitAlyzer1000's receiver, errors are identified by bit-by-bit comparing of the incoming data stream with the expected sequence. Errors found in the received sequence cause error location events to be analyzed in real-time by the internal processor and/or recorded to the internal hard disk drive. Recorded error event streams can be analyzed in a post-processing step just as if they were being taken off a live-input data channel. In addition to complete documentation of test results, recorded error analysis provides the added convenience of being able to change settings between analyses to fully explore all error statistics.

The standard BitAlyzer1000 provides the following analyses:

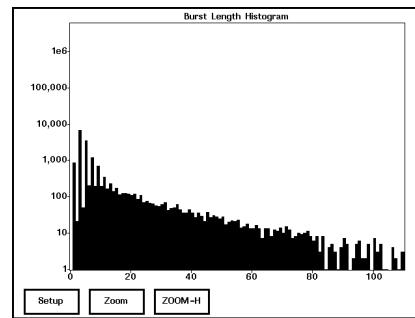
- Total, Bit and Burst Error Rates and Counts
- Strip Chart of Error Rates
- Burst Length Histogram
- Histogram of Error Free Intervals
- Distribution of Error Occurrences per Block

## EXAMPLE ANALYSIS



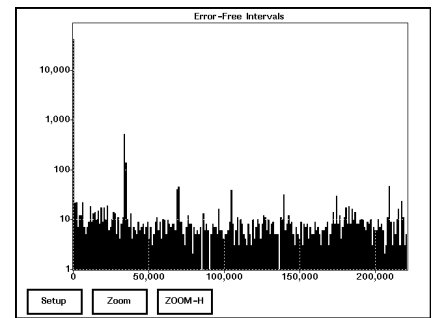
**Strip Chart**

The strip chart display plots the Total BER, Bit BER and Burst BER versus the number of bits that have been received. The integration period to wait between measurements is selectable. You have control over flexible panning and zooming functions and can set up titles, cursors, and grid lines.



**Burst Length Profile**

The burst length profile is a histogram of the number of occurrences of error events of varying lengths. The lengths are measured in bits. The maximum error free interval that can occur within an error burst event can be specified. The analysis can be printed or output to an electronic .PCX image format suitable for importing into other popular software packages.



**Histogram of Error Free Intervals**

Error free intervals indicate a systematic nature of error distribution, often caused by errors that are correlated to data patterns or data formatting operations. A histogram of the bit intervals between errors is provided in the BitAlyzer1000. By using the Zoom button, the histogram will fill the entire screen, allowing easy viewing.

- Error Correlation to external marker input
- Histogram of Pattern Sensitivity
- Multi-channel BER measurements in TDMA formats
- Error Autocorrelation

Bit and burst errors are identified by the local density of errors found near one another. These thresholds are user-definable. Block statistics are based on a flexible user-selected block size that can be used to represent seconds, tracks, rotations, sectors, or tape footage, as needed by a specific application. The error rates are calculated based on dividing the error counts by the total number of bits at a user-selectable integration period.

### ERROR MAPPING AND ECC

Advanced applications found in the BitAlyzer1000 include the ability to image errors found in a data stream onto a user-defined two-dimensional error map as well as Error Correction Coding (ECC) emulation support. Error mapping analysis provides complete pan/zoom and error-size threshold

tools to allow for easy understanding of error phenomena and their relationships to other errors and communication packets or storage sectors. ECC emulation allows users to prototype interleaving, one- and two-dimensional block code ECC strategies on uncorrected channels to evaluate hypothetical performance before formats and real hardware are available.

### 4-MBIT USER PATTERN MEMORY

By augmenting the standard pseudo-random test sequences with user-definable 4-Mbit patterns, the BitAlyzer can emulate special data sequences that more closely match in-service use. User patterns are synchronized by supplying an external Begin Detect input, or by specifying the number of words that makes up one contiguous cycle of the test pattern.

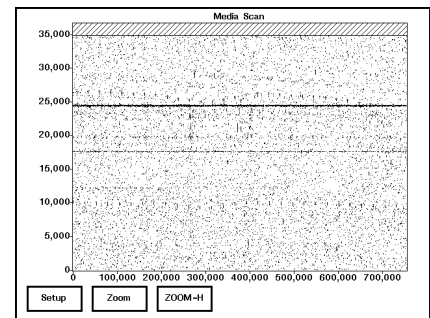
### OPTIONS

#### 16-Mbit User Pattern Memory

Upgrades memory to 16 Mbits for longer user patterns.

### Media Scan Error Map

Media scan creates a two-dimensional image map of errors that corresponds to the transmission format or recording media used. The number of bits per Y-axis "block" is defined by supplying the block size or by using the Marker input. Panning, zooming, error-size thresholds, and cursors allow complete investigation.



### Error Correction Coding

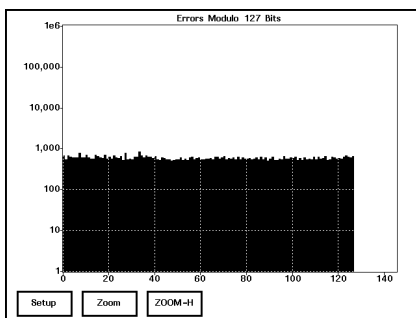
ECC emulation can be used to specify the number of tables, rows and columns to interleave over, and to set the correction strength in both row and column dimensions. It supports using inner code failures as outer code erasures and allows logging error corrector statistics during analysis. Resulting analysis shows the hypothetical error performance of channels using the defined error corrector.

### Stand Alone Analysis Software

Error data sets captured with a BitAlyzer1000 can be analyzed on a Pentium-class computer. This allows for easy in-office analysis as well as for sharing equipment.

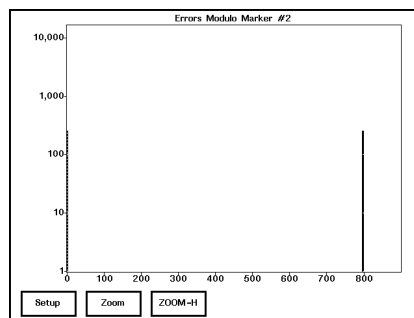
### Auxiliary Bit Error Rate Tester

Two bit error rate testers can be integrated into the BitAlyzer1000 instrument to allow additional simultaneous generation and simple bit error rate measurements at speeds up to 25 Mbit/sec. Ideal for applications where low data rate paths must be tested simultaneously with a high data rate path, the AuxBERT provides serial clock and data interfaces.



**Pattern Sensitivity**

Pattern sensitivity analysis creates a histogram where each bin location corresponds to a bit position in the repeating data sequence. Exact bit error locations are accumulated for each bit position, showing the probability of error in each position of the data sequence. Correlations like this can also be done on any type of repeating sequence by using Modulo-N analysis.



**Modulo Marker Histogram**

Modulo analysis accumulates the number of errors that occur in exact bit locations modulo a user-supplied divisor or an externally applied marker input. Two markers are provided, allowing analysis to be correlated to external events such as format packet boundaries, sectors, or electromechanical dependencies.

## SPECIFICATIONS

Data Rate .....	1000 Mbit/sec maximum
Data Formats .....	Serial, 8-bit and 16-bit parallel
Data Types .....	Pseudo Random: $2^n - 1$ where $n = 7, 15, 20, 23$ 16-bit user-programmed 4-Mbit RAM 16-Mbit RAM ( <i>option</i> )
Logic Levels .....	Serial: ECL Parallel: Differential ECL
Measurements .....	Total, Bit and Burst errors and rates Burst events and rates Total Markers Total Blanks Tx/Rx clock rates
Error Analysis .....	BER Measurements Burst Length Profile Histogram of Error Free Intervals Modulo-N Analysis (max. $N = 4.29 \times 10^9$ ) Modulo-Marker Analysis Modulo-Pattern Period Analysis Strip Chart Block-Mode Analysis Error Autocorrelation Multi-Channel TDMA BER Analysis 2-D Error Mapping ( <i>option</i> ) Error Correction Coding Analysis ( <i>option</i> )
Error Event Storage .....	At least 170 Million Events
Remote Interface .....	IEEE-488 or RS-232C
Mainframe .....	640 x 480 color display, 1.44 MByte MS-DOS compatible floppy

## ORDERING INFORMATION

BA1000 .....	BitAlyzer1000 Error Analyzer
BA1GECC .....	ECC Emulation Package
BA1GRAM16 .....	16 Mbit Fixed Pattern Memory
BA1GCLOCK .....	Internal Clock Synthesizer
BA1GMEDIA .....	Media Scan Analysis Package
BA1GRACK .....	Rack Mount Hardware
BA1GDUT .....	Device Under Test Control Software
BA1GBERT .....	2-Channel Auxiliary Track BERT
BA3YR .....	2 Years Added to Standard 1-Year Warranty

## WARRANTY

All equipment is fully warranted for one year. This includes hardware repair or replacement, at SyntheSys Research's discretion, and software updates. Necessary repairs are performed at the Menlo Park, California factory.

## THE COMPANY

Founded in 1989, SyntheSys Research, Inc. is a manufacturer of test instruments for analyzing a variety of digital communications channels. From fiber optics to satellites, hard disks to laser communications, and HDTV to digital television, the company has pioneered innovative techniques into award-winning, user-friendly instruments. SyntheSys Research is driven by the goal of creating quality products needed by industry professionals.

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