BERTScope™ and BERTScope™ S Signal Integrity Analyzers

Technical Specifications

Benefits:

- Integrated Signal Integrity Analyzer using the same acquisition circuitry for time, error and jitter domain measurements, to give "same observer" measurements that tie together for faster troubleshooting of your problem devices.
- Unique analysis toolkit gives you unrivaled information quality and depth
- 12.5 Gb/s and 7.5 Gb/s (upgradeable) models will cover your needs as your application bit rates increase

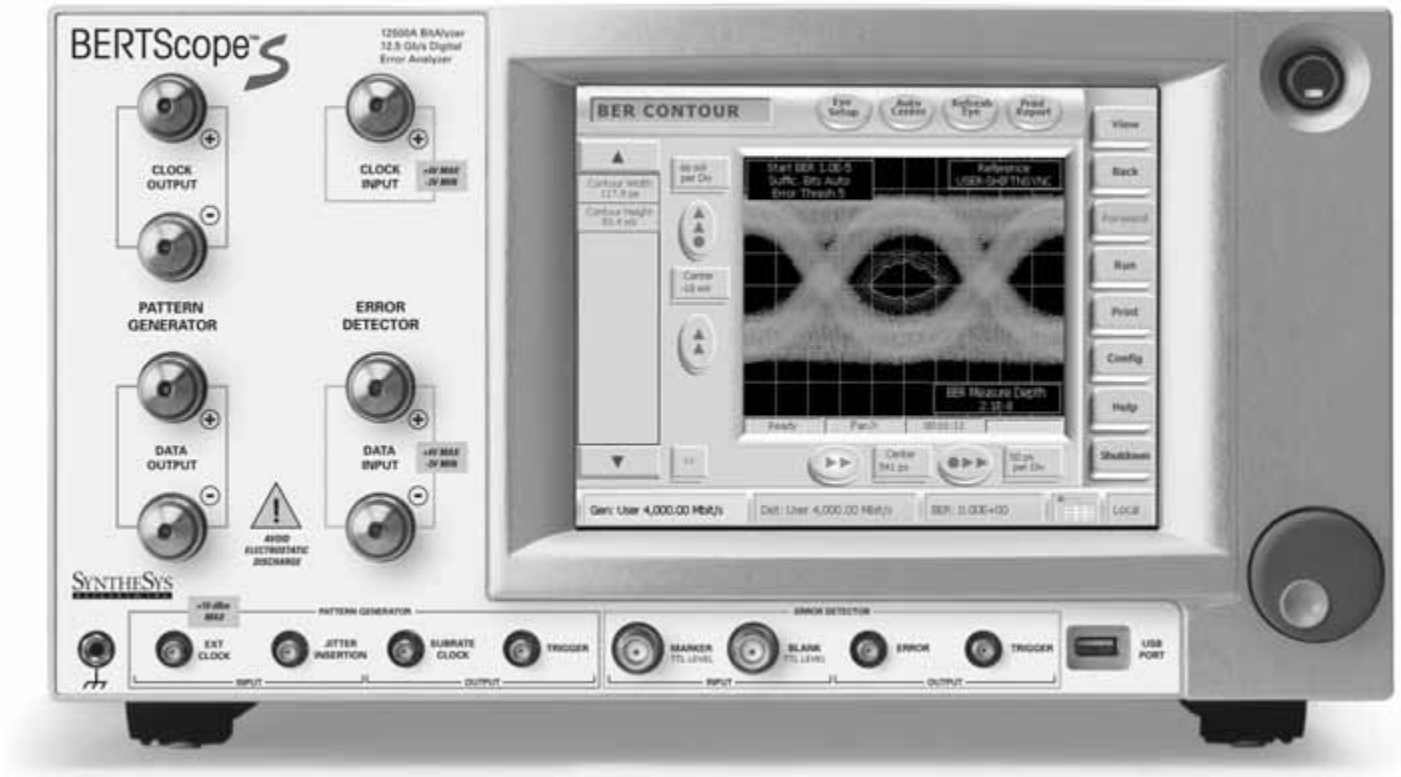
Applications:

- Serial Bus Design
- Semiconductor IC evaluation
- Jitter Tolerance Compliance Testing
- High Speed Backplane Design
- Optical Transceiver Design and Manufacturing
- Recirculating Fiber Loop Experiments

BERTScope and BERTScope S

Technical Specifications

Contents



Pattern Generator
Input/ Output Specifications

Clock and $\overline{\text{Clock}}$ Outputs

Maximum Frequency:	7.5 Gb/s (BSA7500A) 12.5 Gb/s (BSA 12500A)
Minimum Frequency:	500 Mb/s
Internal Clock Phase Noise:	< –90 dBc/Hz @ 10 kHz offset (typical)

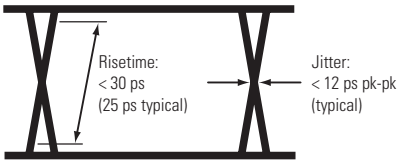
Data and $\overline{\text{Data}}$ Outputs

Format:	NRZ
Polarity:	Normal or Inverted
Variable Crossover:	Supported
Patterns:	
Hardware Patterns:	
Industry standard Pseudo-Random (PRBS) of the following types: $2^n - 1$ where n = 7, 11, 15, 20, 23, 31	
RAM Patterns:	
User-defined:	128 bits to 8 Mbits Two 4 Mbit A/B pages 128-bit word size
Library:	Wide variety including SONET/SDH, Fibre Channel-based such as k28.5, CJTPAT; 2^n patterns where n = 3, 4, 5, 6, 7, 9; Mark Density patterns for 2^n where n = 7, 9, 23; and many more.
Error Insertion:	
Length:	1, 2, 4, 8, 16, 32, 64, 128 bit bursts
Frequency:	Single or repetitive

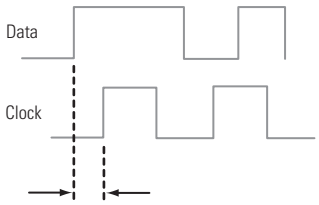
Data/$\overline{\text{Data}}$, Clock/$\overline{\text{Clock}}$ Amplitudes and Offsets

Configuration:	Differential Outputs, each side of pair individually settable for termination, amplitude, offset.
Interface:	DC Coupled, 50 Ω reverse terminated, APC-3.5 connector. Calibration into 75 Ω selectable, other impedances by keypad entry. User-replaceable Planar Crown® adapter allows change to other connector types.
Preset Logic Families:	LVPECL, LVDS, LVTTL, CML, ECL, SCFL
Terminations:	Variable, –2 to +2V. Pre-sets: +1.5, +1.3, +1, 0, –2 V, AC-Coupled
Allowable Amplitudes, Terminations, and Offsets:	See Figures 1 and 2

Data/$\overline{\text{Data}}$, Clock/$\overline{\text{Clock}}$ Waveform Performance



Clock/Data Delay



Range:

Up to 1.1 GHz	30 ns
Above 1.1 GHz	3 ns

(Greater than 1 bit period in all cases)
Resolution: 100 fs
Self-Calibration:
Supported – at time of measurement, when temperature or bit rate are changed, instrument will recommend a self calibration. Operation takes less than 10 seconds.

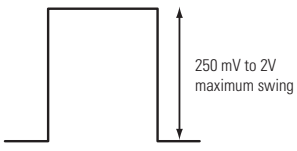


Figure 1. Amplitude range.

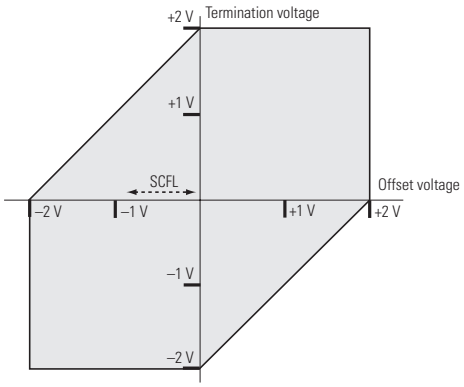


Figure 2. Allowable combinations of termination and offset. Amplitude swings between 0.25 and 2 V allowed; should fit inside shaded area of graph. For example, SCFL uses a 0 V termination, and operates between approximately 0 and –0.9 V; as shown with dotted arrow, it falls within the operating range.

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Pattern Generator Ancillary Connections

Front Panel Pattern Generator Connections

External Clock Input

Allows use of an external clock source to clock the BERTScope.

Frequency Range:	0.5 to 12.5 GHz
Nominal Power:	+3 dBm
Maximum Power:	+10 dBm
Return Loss:	Better than –6 dB
Interface:	50 Ω SMA female, DC coupled to selectable termination.

Trigger Output

Provides a pulse trigger to external test equipment. It has two modes:
1. Divided Clock Mode: Pulses at 1/256th of the clock rate
2. Pattern Mode: Pulse at a programmable position in the pattern (PRBS), or fixed location (RAM patterns)

Minimum Pulse Width:	128 Clock Periods (Mode 1) 512 Clock Periods (Mode 2)
Transition Time:	< 500 ps
Jitter (p-p, data to trigger)**:**	< 100 ps
Output Levels:	> 300 mV amplitude, 650 mV offset
Interface:	50 Ω SMA female, DC coupled to 0 V

Jitter Insertion (Stressed Eye Option)

Part of the Stressed Eye Option, one of two jitter insertion inputs. Can be used to insert SJ, RJ, BUJ if desired.

Frequency Range:	DC to 1.0 GHz
Jitter Amplitude Range:	Up to 0.5 UI (max.)
Voltage Range:	to +10 dBm approximately (+20 dBm max to avoid damage
Interface:	50 Ω SMA female, DC coupled to 0 V

Sub-Rate Clock Output

Clock divided by 4. With Option SE fitted, clock divided ratios available are as follows: 1, 2, 4, 8, 16, 32, 64, 128.Output is low jitter, even when clock output is modulated by Stressed Eye Option.

Frequency Range:	0.125 to 3.125 GHz
Amplitude Range:	1V nominal, centered around 0 V
Transition Time:	< 500 ps
Interface:	50 Ω SMA female, DC coupled to 0 V

Rear Panel Pattern Generator Connections

See next page

Pattern Start Input

For users wanting to synchronize patterns of multiple data streams from multiple instruments simultaneously.

Logic Levels:	LVTTL (< 0.5 V Lo, > 2.5 V hi)
Threshold:	+1.2 V typical
Minimum Pulse Width:	128 serial clock periods
Maximum Repetition Rate:	512 serial clock periods
Interface:	SMA female, > 1 kΩ impedance to 0 V

Sinusoidal Jitter Input (Stressed Eye Option)

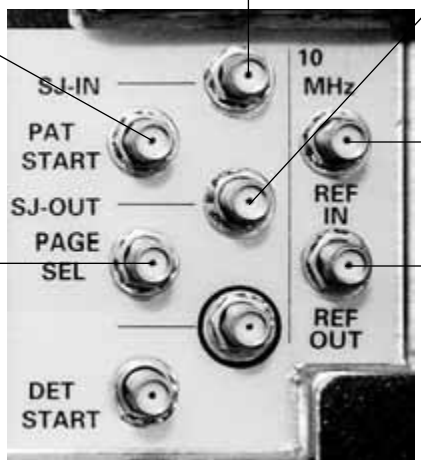
Allows use of external low frequency sinusoidal jitter source to modulate the stressed eye option.

Frequency Range:	DC to 80 MHz
Jitter Amplitude Range:	Up to 1ns
Voltage Range:	to +10 dBm approximately (+20 dBm max to avoid damage
Interface:	SMA female

Sinusoidal Jitter Output

(Stressed Eye Option)
To allow phasing of two BERTScopes together, in-phase or anti-phase.

Frequency:	As set for internal SJ from GUI
Amplitude:	2 V p-p
Interface:	SMA female,



Page Select Input

In A-B Page Select Mode, allows external control of pattern. Pulse Hi causes instance(s) of Pattern B.

Logic Levels:	LVTTL (< 0.5 V Lo, > 2.5 V hi)
Threshold:	+1.2 V typical
Minimum Pulse Width:	1 pattern length
Interface:	SMA female, > 1 kΩ impedance to 0 V

10 MHz Reference Input

To lock the BERTScope to the 10 MHz reference of another piece of equipment.

Frequency:	10 MHz
Amplitude:	0 dBm
Interface:	50 Ω SMA female, DC coupled to 0 V

10 MHz Reference Output

To allow the BERTScope to act as the 10 MHz reference that other equipment is locked to.

Frequency:	10 MHz
Amplitude:	250 mV p-p, nominal
Interface:	50 Ω SMA female, DC coupled to 0 V

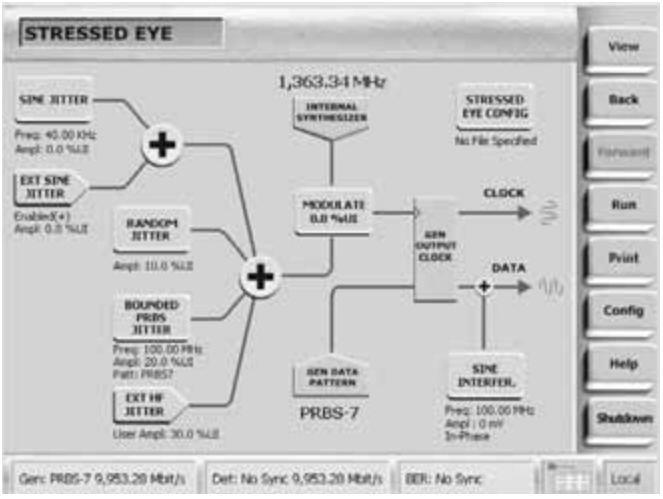
Pattern Generator Stressed Eye

Generator Option

- Flexible, integrated stressed eye impairment addition to the internal clock
- Easy set-up, with complexity hidden from the user with no loss of flexibility
- Verify compliance to multiple standards using the BERTScope and external ISI filters. Standards such as:
  - OIF CEI
  - Serial-ATA II
  - PCI-Express
  - XFI
- Sinusoidal interference may be inserted in phase or in anti-phase
- Sinusoidal jitter may be locked between two BERTScopes in phase or anti-phase, as required by OIF CEI

Flexible External Jitter Interfaces:

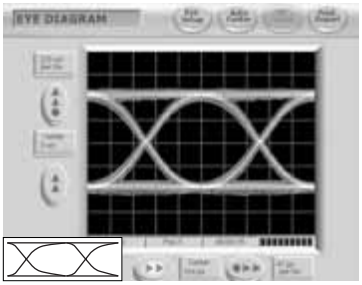
- Front Panel External High Frequency Jitter Input Connector – Jitter from DC to 1.0 GHz up to 0.5 UI (max.) may be added, of any type that keeps with amplitude and frequency boundaries.
- Rear Panel External SJ Low Frequency Jitter Input Connector – Jitter from DC to 80 MHz up to 1ns (max) may be added
- Rear Panel SJ Output



Notes: Specified for data rates from 1.5 Gb/s to 11.2 Gb/s. Usable with limited performance to 622 Mb/s.
Internal RJ, BUJ, and external jitter input limited to 0.5 UI, combined.

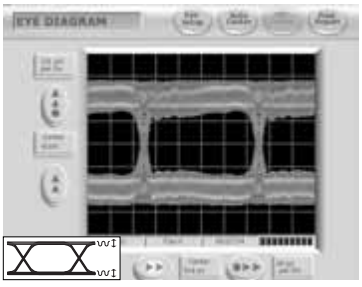
Amplitude & ISI Impairments

ISI



Add externally: For example long coax cable length, or Bessel-Thompson 4th Order Filter with –3 dB point at 0.75 of Bit Rate etc.

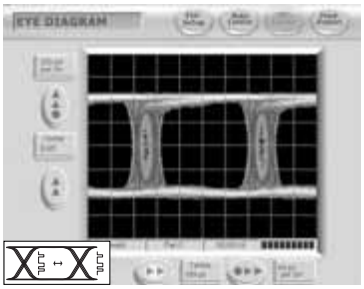
Sinusoidal Interference



- 100 MHz to 2.5 GHz
- Adjustable in 100 kHz steps
- Adjustable relative to data magnitude from 0 to 400 mV
- Common mode or differential

Jitter Impairments

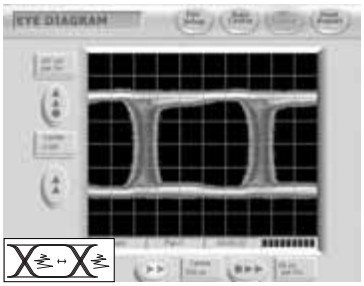
Bounded Uncorrelated Jitter



- Internal PRBS Generator PN-7
- Variable up to 0.5 UI
- 100 Mb/s to 2.0 Gb/s
- Band limited by selected filters – see table below:

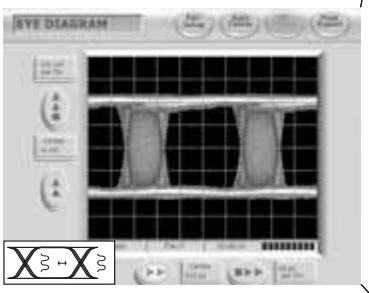
BUJ Rate	Filter (MHz)
100 to 499	25
500 to 999	50
1,000 to 1,999	100
2,000	200

Random Jitter



- Variable up to 0.5 UI
- Band limited 10 MHz to 1 GHz

Sinusoidal Jitter



Data Rate	Internal SJ Frequency Range	
	1kHz to 10 MHz	10 MHz to 80 MHz
10.3125 Gb/s	0 to 9.2 UI	0 to 0.5 UI
9.9545 Gb/s	0 to 8.9 UI	0 to 0.5 UI
8.5 Gb/s	0 to 7.6 UI	0 to 0.5 UI
6.25 Gb/s	0 to 5.6 UI	0 to 0.5 UI
6 Gb/s	0 to 5.4 UI	0 to 0.5 UI
5 Gb/s	0 to 4.5 UI	0 to 0.5 UI
4.25 Gb/s	0 to 3.8 UI	0 to 0.5 UI
3.125 Gb/s	0 to 2.8 UI	0 to 0.5 UI
3 Gb/s	0 to 2.7 UI	0 to 0.5 UI
2.5 Gb/s	0 to 2.2 UI	0 to 0.5 UI
2.4883 Gb/s	0 to 2.2 UI	0 to 0.5 UI
2.125 Gb/s	0 to 1.9 UI	0 to 0.5 UI
1.5 Gb/s	0 to 1.35 UI	0 to 0.5 UI

SJ adjustable from 0 to levels greater than or equal to range in table.

Error Detector

Clock and Data Inputs

Clock Input

Maximum Frequency: 12.5 Gb/s (BSA 12500A & 7500A)
Minimum Frequency: 500 Mb/s

Data and $\overline{\text{Data}}$ Inputs

Format: NRZ
Polarity: Normal or Inverted
Threshold: Manually adjustable from –2.4 V to +2.5 V, or automatically with Auto-Align
Sampling: Clock rising edge
Sensitivity:
Single-Ended 100 mV p-p (typical)
Differential: 50 mV p-p (typical)
Maximum input Signal Swing: 2 V p-p

Patterns:

Hardware Patterns:
Industry standard Pseudo-Random (PRBS) of the following types: $2^n - 1$ where n = 7, 11, 15, 20, 23, 31

RAM Patterns:
User-defined: 128 bits to 8 Mbits 128-bit increments
Library: Wide variety including SONET/SDH, Fibre Channel-based such as k28.5, CJTPAT; 2^n patterns where n = 3, 4, 5, 6, 7, 9; Mark Density patterns for 2^n where n = 7, 9, 23; and many more.

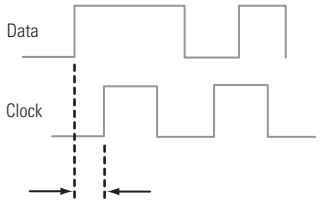
RAM Pattern Capture: Capture incoming data up to 8 Mbit in length. Edit captured data, send to Pattern Generator, Error Detector or both.

Modes:
Capture by Length: 1 to 262,143 words, 1 word default. Words 128 bit in length.
Capture by Triggers: Captures when "Detector Start" on rear panel goes high, to maximum allowable length or until input goes low.
Capture by Length from Trigger: Capture by length initiated from Detector Start input, to pre-specified length.

Data/$\overline{\text{Data}}$, Clock Interfaces

Configuration: Differential data input. Single-ended clock input, settable for amplitude, offset.
Interface: APC-3.5 connector. Calibration into 75 Ω selectable. Selectable Single-ended, single-ended inverted, differential
Preset Logic Families: LVPECL, LVDS, LVTTL, CML, ECL, SCFL
Terminations: Variable, –2 V to +2 V. Pre-sets: +1.5, +1.3, +1, 0, –2 V, AC-Coupled

Clock/Data Delay



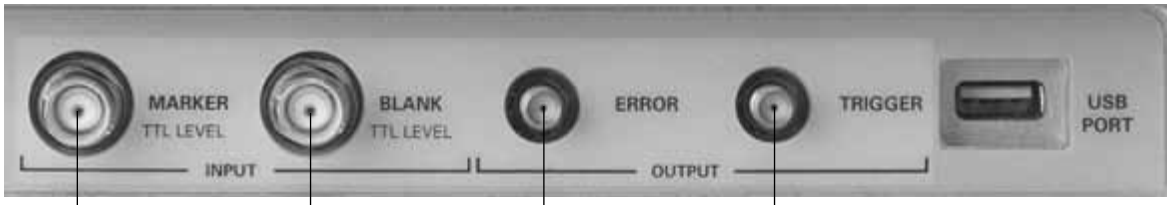
Range:
Up to 1.1 GHz 30 ns
Above 1.1 GHz 3 ns
(Greater than 1 bit period in all cases)
Resolution: 100 fs
Self-Calibration:
Supported – at time of measurement, when temperature or bit rate are changed, instrument will recommend a self calibration. Operation takes less than 10 seconds.

Synchronization:
Auto-Resync: User-specified number of 128 bit words containing 1 or more errors per word initiates a re-sync attempt.
Manual: User initiates re-sync
Pattern Matching:
Grab 'n' Go Error Detector captures specified pattern length and compares next instances to find match. (Fast method, but susceptible to ignoring logical errors.)
Shift-to-Sync Error Detector compares incoming pattern with reference RAM pattern, looks for match, if none found, shifts pattern by one bit and compares again.(Slower but most accurate method.)

Error Detector Basic Measurements: BER, Bits Received, Re-Syncs, Measured Pattern Generator and Error Detector clock frequencies

Error Detector Ancillary Connections

Front Panel Error Detector Connections



Error Correlation Marker Input
(Error Analysis)
Allows an external signal to provide a time-tagged marker to be placed in the error data set.

Logic Family:	LVTTL (< 0.5 V Lo, > 2.5 V hi)
Threshold:	+1.2 V
Minimum Pulse Width:	128 Clock Periods
Maximum Repetition Rate:	512 serial clock periods
Maximum Frequency:	< 4000 markers/sec recommended
Interface:	BNC female, > 1 KΩ impedence to 0 V

Blank Input
Useful for re-circulating loop fiber experiments. Causes errors to be ignored when active. Bit count, error count & BER not counted. No re-sync occurs when counting re-enabled.

Logic Family:	LVTTL (< 0.5 V Lo, > 2.5 V hi)
Threshold:	+1.2 V
Minimum Pulse Width:	128 Clock Periods
Maximum Repetition Rate:	512 serial clock periods
Interface:	BNC female, > 1 KΩ impedence to 0 V

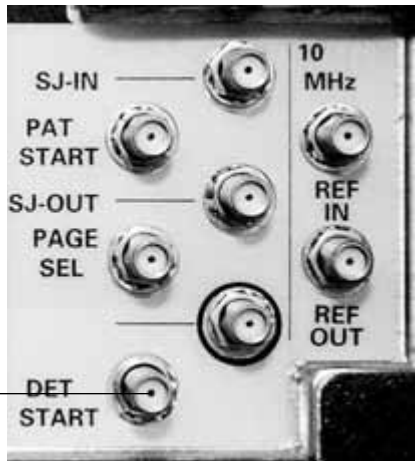
Trigger Output
Provides a pulse trigger to external test equipment. It has two modes:
1. Divided Clock Mode: Pulses at 1/256th of the clock rate
2. Pattern Mode: Pulse at a programmable position in the pattern (PRBS), or fixed location (RAM patterns)

Minimum Pulse Width:	128 Clock Periods (Mode 1) 512 Clock Periods (Mode 2)
Transition Time:	< 500 ps
Jitter (p-p, data to trigger)**:**	< 100 ps
Output Levels:	> 300 mV amplitude, 650 mV offset
Interface:	50 Ω SMA female, DC coupled to 0 V

Error Output
Provides a pulse when an error is detected. Useful for triggering an alarm while doing long-term monitoring, etc.

Minimum Pulse Width:	128 Clock Periods
Transition Time:	< 500 ps
Output Levels:	1000 mV nominal (0 V to 1 V low-high)
Interface:	50 Ω SMA female, DC coupled to 0 V

Rear Panel Error Detector Connections



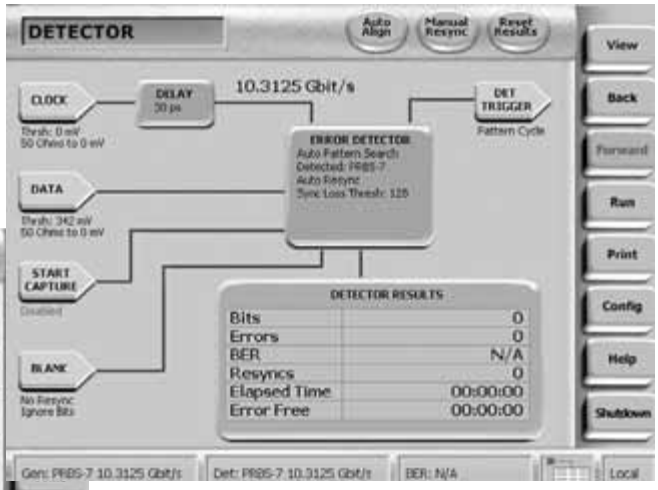
Detector Start Input
Used to trigger the acquisition of incoming data into the Error Detector reference pattern memory. High level starts capture.

Amplitude:	LVTTL (< 0.5 V Lo, > 2.5 V hi)
Threshold:	+1.2 V
Minimum Pulse Width:	128 serial clock periods
Maximum Repetition Rate:	512 serial clock periods
Interface:	SMA female, > 1kΩ impedance to 0 V

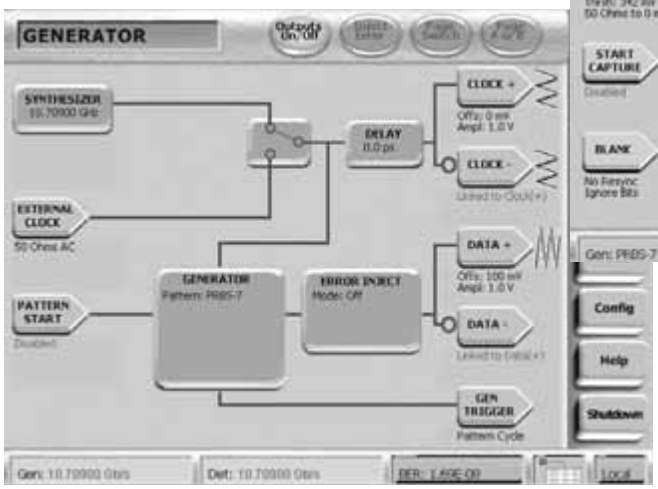
User Interfaces

Taking Usability to New Heights

- Easy navigation
- Logical layout and operation
- Multiple ways of moving between screens
- Relevant information right where you need it
- Color-coding to alert you to the presence of non-standard conditions



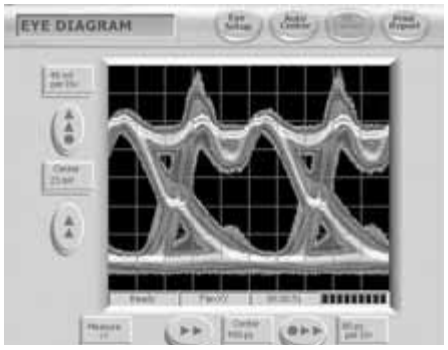
Error Detector Set-Up Screen

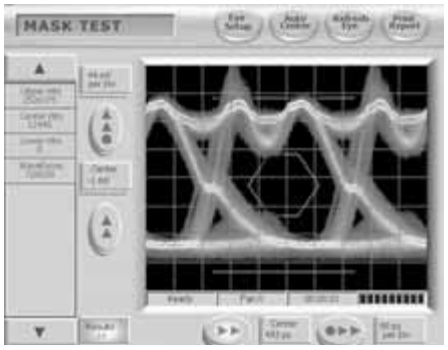


Pattern Generator Set-Up Screen

Editor Screen

- Used for pattern editing of standard and AB Page Select patterns, also mask editing
- Views in Binary, Decimal or Hexadecimal
- Support for variable assignments, repeat loops, seeding of PRBS patterns
- Capture and editing of incoming data - for example, to make a repeating pattern out of real-world traffic.





BERTScope Built-In Parametric Measurements

All BERTScopes come with Eye Diagrams and Mask Test capabilities as standard, along with Error Analysis.

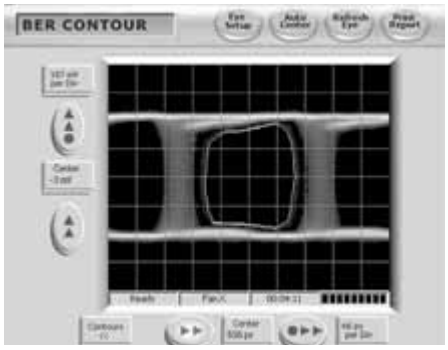
Eye Diagram

- 280x350 pixel waveform display
- Deep acquisition
- Automatic Measurements include:
  - Rise Time
  - Fall Time
  - Unit Interval (Data, and also Clock)
  - Eye Amplitude
  - Noise Level of 1 or 0
  - Eye Width
  - Eye Height
  - Eye Jitter (p-p and RMS)
  - 0 Level, 1 Level
  - Extinction Ratio
  - Vertical Eye Closure Penalty (VECP)
  - Dark Calibration
  - Signal to Noise Ratio
  - Vp-p, Vmax, Vmin, Crossing Levels

Mask Testing

- Library of standard masks e.g. XFP, or edit custom masks
- Addition of positive or negative mask margin
- Import of measured BER Contour to become process control mask
- At least 1000x the sample depth of traditional sampling oscilloscope masks is ideal for ensuring the absence of rare event phenomena.

Physical Layer Test Option

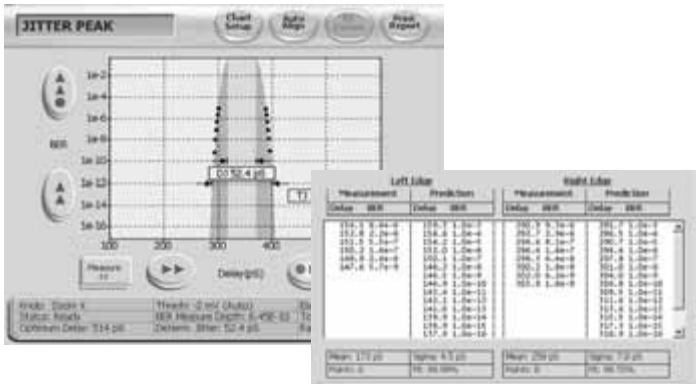


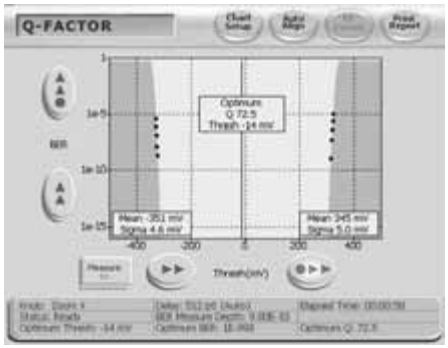
BER Contour Testing

- Executed with same acquisition circuitry as Eye Diagram measurements for maximum correlation
- As-needed delay-calibration for accurate points
- Automatic scaling, one button measurement
- Extrapolates contours from measured data, increasing measurement depth with run-time and repeatedly updating curve-fits
- Easy export of fitted data in CSV format
- Contours available from 10^{-6} to 10^{-16} in decade steps

Jitter Measurements

- Testing to T11.2 MJSQ BERTScan methodology (also called 'Bathtub Jitter')
- Deep measurements for quick and accurate extrapolation of Total Jitter at user-specified level, or direct measurement
- Separation of Random and Deterministic components, as defined in MJSQ
- As-needed delay-calibration for accurate points
- Easy export of points in CSV format
- Easy one-button measurement
- User-specified amplitude threshold level, or automatic selection
- Selectable starting BER to increase accuracy when using long patterns, as defined in MJSQ





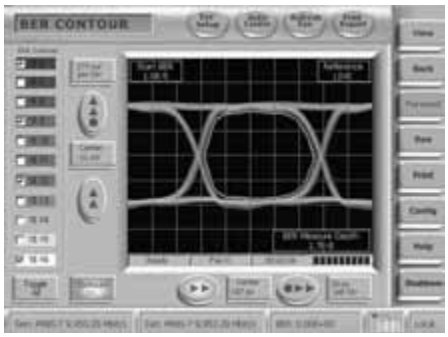
Q Factor Measurement

- One-button measurement of a vertical cross-section through the middle of the eye.
- Easy visualization of system noise effects
- Export of data in CSV format

Compliance Contour

- Validation of transmitter eye performance to standards such as XFP/XFI and OIF CEI.
- Overlay compliance masks onto measured BER contours and easily see whether devices pass the BER performance level specified.

Live Data Analysis Option



The live data option is designed to measure parametric performance of traffic that is either unknown, or non-repeating. This can include traffic with idle bits inserted such as in systems with clock rate matching. It is also suitable for probing line cards etc.

The option uses one of the two front-end decision circuits to decide whether each bit is a one or zero by placing it in the center of the eye. The other is then used to probe the periphery of the eye to judge parametric performance. This method is powerful for physical layer problems, but will not identify logical problems due to protocol issues, where a zero was sent when it was intended to be a one.

Live data measurements can be made using BER Contour, Jitter Peak, Q Factor. Eye diagram measurements can be made on live data without the use of this option, providing a synchronous clock is available.

The Live Data Analysis option requires the Physical Layer Test Option.

Error Analysis

Error analysis is a powerful series of views that associate error-occurrences so that underlying patterns can be easily seen. It is easy to focus in on a particular part of an eye diagram, move the sampling point of the BERTScope there, and then probe the pattern sensitivity occurring at that precise location. For example, it is straightforward to examine which patterns are responsible for late or early edges.

Many views come standard with the BERTScope family.

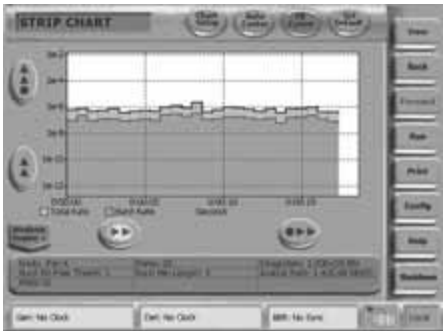
Analysis Views

- **Error Statistics:** A tabular display of bit and burst error counts and rates.
- **Strip Chart:** A strip chart graph of bit and burst error rates.
- **Burst Length:** A histogram of the number of occurrences of errors of different lengths.
- **Error Free Interval:** A histogram of the number of occurrences of different error free intervals.
- **Correlation:** A histogram showing how error locations correlate to user-set block sizes or external Marker signal inputs.
- **Pattern Sensitivity:** A histogram of the number of errors at each position of the bit sequence used as the test pattern.
- **Block Errors:** A histogram showing the number of occurrences of data intervals (of a user-set block size) with varying numbers of errors in them.

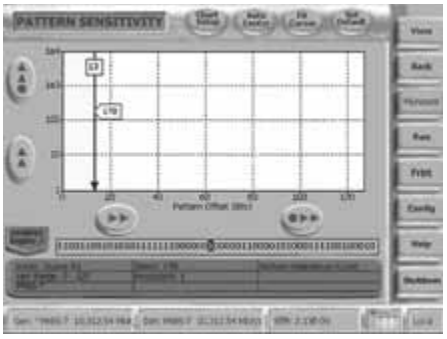
Error Location Capture

Live Analysis	Continuous
Error Logging Capacity	Max. 2 GB file size
Error Events/Second	10,000
Maximum Burst Length	32 kbits

Error Statistics View showing link performance in terms of bit and burst occurrences.



Viewing bit and burst error performance over time. This can useful while temperature cycling as part of troubleshooting, for example.



Pattern Sensitivity is a powerful way of examining whether error events are pattern related. It shows which pattern sequences are the most problematic, and operates on PRBS and user-defined patterns.

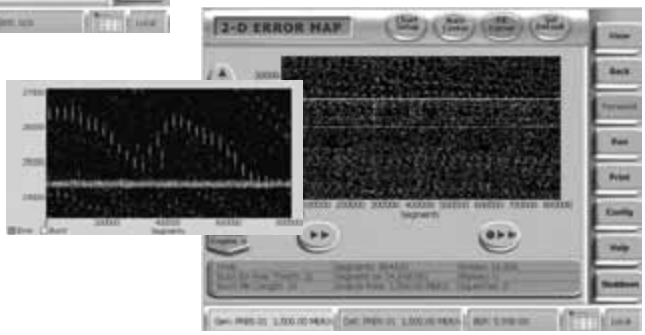
Error Analysis Options

Forward Error Correction Emulation

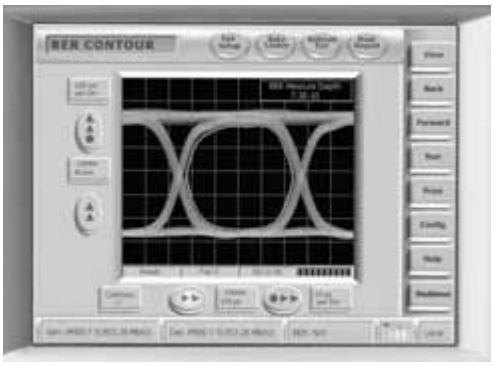
Because of the patented error location ability of the BERTScope, it knows exactly where each error occurs during a test. By emulating the memory blocks typical of block error correcting codes such as Reed-Solomon architectures, bit error rate data from uncorrected data channels can be passed through hypothetical error correctors to find out what a proposed FEC approach would yield. Users can set up error correction strengths, interleave depths, and erasure capabilities to match popular hardware correction architectures.

2-D Error Mapping

This analysis creates a two-dimensional image of error locations from errors found during the test. Error mapping based on packet size or multiplexer width can show if errors are more prone to particular locations in the packet or particular bits in the parallel bus connected to the multiplexer. This visual tool allows for human eye correlation, which can often illuminate error correlations that are otherwise very difficult to find-even with all the other error analysis techniques.



General

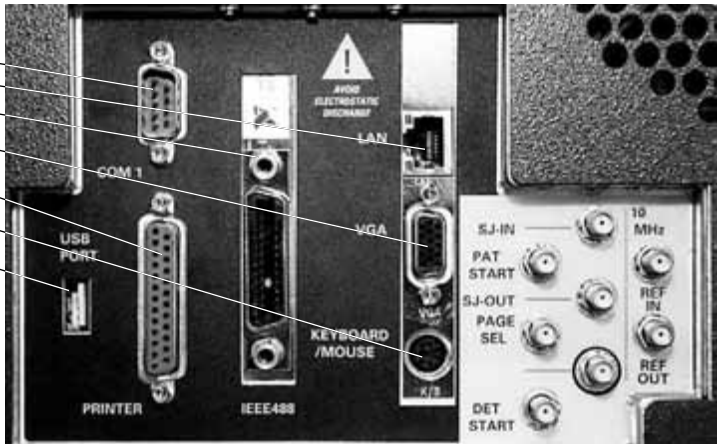


PC-Related:

Display:	TFT Touch Screen 640 x 480 VGA
Touch Sensor:	Analog Resistive
Processor:	1 GHz Pentium or equivalent
Hard Disk:	20 GB or greater
DRAM:	256 MB
Operating System:	Windows 2000
Remote Control:	IEEE-488 (GPIB) or TCP/IP

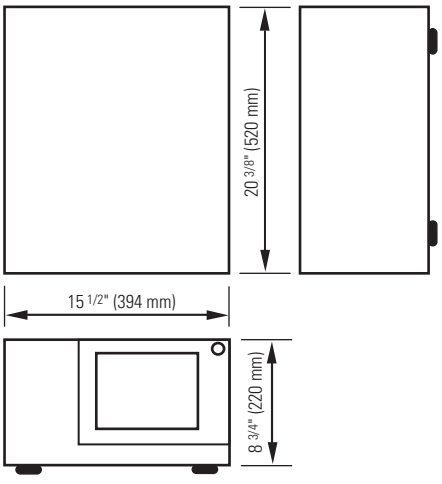
Supported Interfaces:

Serial (RS-232)
Network (100 Base-T RJ-45 Ethernet)
IEEE-488 (GPIB)
Monitor (DB-15 VGA)
Printer Port (Centronix)
Keyboard (Micro)
Mouse (PS/2)
USB 1.0 (1 front panel, 1 rear panel)



Physical:

Power:	< 400 Watts
Voltage:	90 to 240 V AC, 50 to 60 Hz
Weight:	55 lbs (25 kg)
Dimensions:	8 3/4" (H) x 15 1/2" (W) x 20 3/8" (D)



Environmental:

Warm-up time:	20 minutes
Operating Temperature Range:	10 to 40 °C
Humidity:	Non-condensing at 40 °C, 15 to 95%
Certifications:	EU EMC Directive (CE-Marked) UL: Underwriters Labs (US) certification CSA (Canada) FCC

Support:

Period:	1 year (extendable to 3 years with orderable option)
Coverage:	Hardware repair or replacement, at SyntheSys Research's discretion. Also covers software updates. Repairs performed at the Menlo Park, California, USA facility.
Calibration interval	1 year

Ordering Information

BERTScope 7500A
7.5 G Pattern Generator, Error Detector, 500 MHz to 7.5 GHz Clock Source, BitAlyzer Error Location Analysis, Eye Diagram Analysis, Mask Test. Upgradeable to BSA12500A for additional charge.

BERTScope 12500A
12.5 G Pattern Generator, Error Detector, Error Location Analysis, 500 MHz to 12.5 GHz Clock Source, BitAlyzer Error Location Analysis, Eye Diagram Analysis, and Mask Test.

BERTScope 12500A, 7500A Stress Analyzer
Powerful stress testing and analysis bundle. Combines Stressed Eye generation (Option SE), Physical Layer Test Suite (Option PL), Error Mapping (Option MAP) and Forward Error Correction (Option FEC) into one convenient and economic bundle.

NOTES
Rise times are measured 20% to 80%. Specifications are following a 20 minute warm up period. Specifications subject to charge.

Options:

BSA7500/12500PL
Physical Layer Test Suite Option including: BER Contour, Q-Factor, Jitter Peak, and Compliance Contour.

BSA7500/12500LDA
Enables measurement of Jitter Peak, BER contour and Q-factor on non-repetitive data such as live traffic and system level traffic with inserted idle bits or added protocol. Requires Physical Layer Test option.

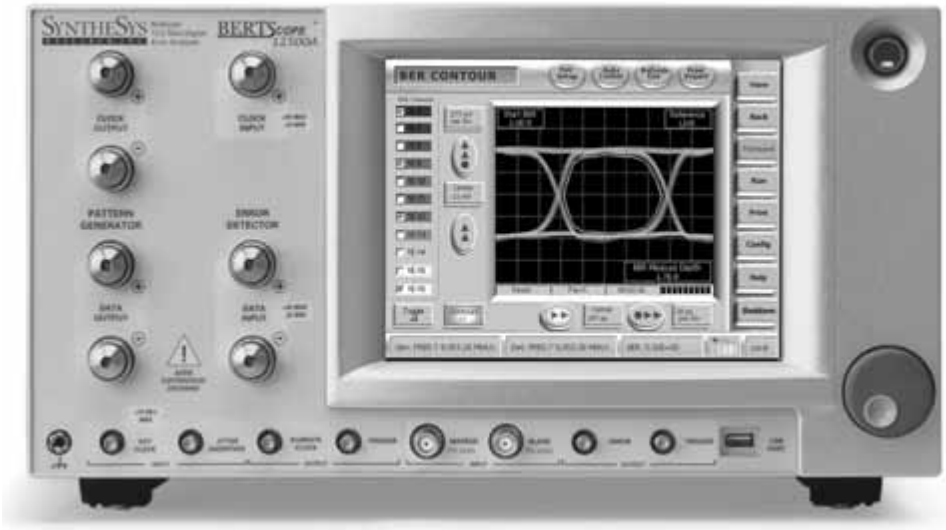
BSA7500/12500SE
Stressed Eye Option. Clock source with calibrated sinusoidal jitter injection for telecom and datacom jitter tolerance testing, together with bounded, uncorrelated jitter and random jitter injection for stressed eye generation.

BSA7500/12500FEC
Forward Error Correction Emulation Option

BSA7500/12500MAP
Error Mapping Analysis Option

BSA12500RACK
Rack Mounting Kit. For applications that require it, the BSA12500A can be conveniently rack-mounted. The attractive brushed-aluminum rack-mount kit includes slides so that the unit can easily be pulled out from the rack. Additionally, there is an access panel below the front of the unit that can be removed to allow convenient cabling access from inside the rack.

BSA12500A3YR
Add 2 Years to Standard 1-Year Warranty. The Extended Warranty option adds a two-year extension to the standard one-year product warranty. All warranties include both hardware repair and software updates. System repair or replacement is at SyntheSys Research's discretion. All repairs are performed at our Menlo Park facility. The warranty includes the cost of ground freight for return shipment. Extended warranties must be ordered within one year of initial delivery.



SYNTHESYS
RESEARCH, INC.

BERTScope™
12.5 Gb/s Signal Analysis

www.bertscope.com

ACCOMPANYING LITERATURE
BERTScope™ Family, brochure, literature number SR-DS013

BERTScope™ Clock Recovery Unit CRU 12500A, brochure and technical specifications, literature number SR-DS016

THE COMPANY
Founded in 1989, SyntheSys Research, Inc. is a manufacturer of test instruments for analyzing a variety of digital communications channels. From fiber optics to satellites, hard disks to laser communications, and HDTV to digital television, the company has pioneered innovative techniques into award winning, user-friendly instruments. SyntheSys Research is driven by the goal of creating quality products needed by industry professionals.

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