1.2.2 Options

Table 1.2.2-1 and Table 1.2.2-2 show the options for the MU181040A/B. Table 1.2.2-3 and Table 1.2.2-4 show the Accessories for options for the MU181040A/B. All options are sold separately.

Table 1.2.2-1 Options for MU181040A

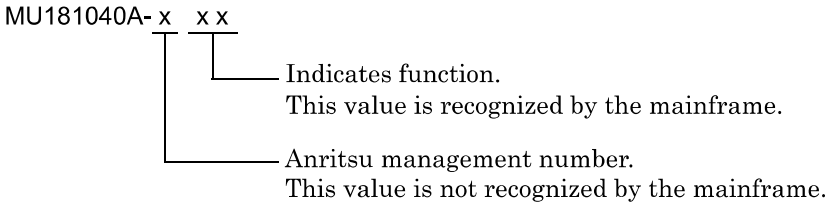
Model name	Product name	Remarks
MU181040A-001	9.8 to 12.5 Gbit/s	Cannot be installed together with MU181040A-002.
MU181040A-002	0.1 to 12.5 Gbit/s	Cannot be installed together with MU181040A-001.
MU181040A-x20	Clock recovery	Can be installed when MU181040A-002 is installed.
MU181040A-x30	Clock phase variable	Can be installed when MU181040A-002 is installed.

Table 1.2.2-2 Options for MU181040B

Model name	Product name	Remarks
MU181040B-002	0.1 to 14 Gbit/s	Necessary option
MU181040B-003	14.05 Gbit/s Extension	
MU181040B-x20	Clock recovery	Can be installed when MU181040B-002 is installed.
MU181040B-x30	Clock phase variable	Can be installed when MU181040B-002 is installed.

Note:

Option name format is as follows:



Notes on MU181040B Option Model Display

The model and name of the MU181040B-003 option are recorded on the front panel of each module. Although the screen displaying the option details using software indicates MU181040B-02 (0.1 to 14 Gbit/s) the assured operating bit rates are actually 0.1 to 14.05 Gbit/s.

1.3.2 Specifications for MU181040B

Table 1.3.2-1 Specifications for MU181040B

Item		Specifications	Remarks
Operating frequency range		0.1 to 14 GHz (When MU181040B-002 is installed) 0.1 to 14.05 GHz (When MU181040B-002 and 003 are installed.)	
Clock source		External clock and Recovered clock can be set.	When MU181040 B-x20 is installed
Rated frequency selection		10GFC over FEC, 10GbE over FEC, OTU2, G975 FEC, 10GFC, 10GbE, OC192/STM64, SATA 6Gb/s, PCI Express II, 4GFC, XAUI, SATA 3Gb/s, OTU1, PCI Express I, OC48/STM16, 2GFC, SATA1.5Gb/s, GbE, 1GFC, OC12/STM4, OC3/STM1 can be set.	
Pattern Sequence		Repeat/Burst	
PRBS	Pattern length	$2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23, 31)	
	Mark ratio	1/2, 1/4, 1/8, 0/8, 1/2 INV, 3/4, 7/8, 8/8	
	Number of AND bit shifts at the mark ratio	1 bit/3 bits (at 1/4, 3/4, 7/8, 1/8)	
Zero Substitution	Pattern sequence	2^n or 2^n-1	
	Additional Bit	1 or 0 (when 2^n is set for Pattern sequence)	
	Pattern length	2^n (n = 7, 9, 10, 11, 15, 20, 23) 2^n-1 (n = 7, 9, 10, 11, 15, 20, 23)	
	Successive-zeros bit length	1 to "pattern length – 1" bits can be inserted.	
Data	Pattern length	2 to 134,217,728 bits, in 1-bit steps In the case of 2 Ch Combination: 4 to 268,435,456 bits, in 2-bit steps In the case of 4 Ch Combination: 8 to 536,870,912 bits, in 4-bit steps	

Table 1.3.2-1 Specifications for MU181040B (Cont' d)

Item		Specifications	Remarks
Mixed	Number of blocks	1 to the smallest number among a to d, below, in 1-block steps a) 511 b) INT (128 Mbits × x/(Number of rows × Data Length')) where Data Length' is: - When Data Length is indivisible by (128 × x) =(INT(Data Length/(128 × x)) +1) × 128 × x - When Data Length is divisible by (128 × x) =Data Length The maximum number of blocks fulfilling the following formula applies: Data Length' × Number of rows × Number of blocks ≤ 128 Mbits c) INT((128 Mbits +2^{31}) × x/(Row Length × Number of rows)) where x is: 1 for Independent 2 for 2 Ch Combination 4 for 4 Ch Combination d) (Row Length – Data Length) × Number of blocks ≥ 2^31(2147483648)	
	Pattern	Data	
	Pattern Length	Data length: 512 to 134,217,728 bits, in 1-bit steps In the case of 2 Ch Combination: 1,024 to 268,435,456 bits, in 2-bit steps (Data) In the case of 4 Ch Combination: 2,048 to 536,870,912 bits, in 4-bit steps (Data) PRBS length: 2^n–1 (n = 7, 9, 10, 11, 15, 20, 23, 31)	
	Row Length	768 to 2,281,701,376 bits, in 128-bit steps In the case of 2 Ch Combination: 1,536 to 4,563,402,752 bits, in 256-bit steps In the case of 4 Ch Combination: 3,072 to 9,126,805,504 bits, in 512-bit steps	

Table 1.3.2-1 Specifications for MU181040B (Cont' d)

Item		Specifications	Remarks
Mixed (continued)	Number of rows	1 to the smallest number among a to c, below, in 1-row steps a) 16 b) INT (128 Mbits × x/Data Length') where Data Length' is: - When Data Length is indivisible by (128 × x) =(INT(Data Length/(128 × x))+1)× 128 × x - When Data Length is divisible by (128 × x) =Data Length The maximum number of rows fulfilling the following formula applies: Data Length' × Number of rows × Number of blocks ≤ 128 Mbits c) INT((128 Mbits +2^{31})× x/Row Length) where x is; 1 for Independent 2 for 2 Ch Combination 4 for 4 Ch Combination	
Sequence	Block number	1 to 128 max.	
	Block length	1,6384 to 1,048,576 bits, in 128-bits steps	
	Loop time	1 to 1,024 times, in 1-time steps or repeat	
Match Pattern		4 to 64 bits per pattern A or B, in 1-bit steps (Settable for each block)	
Block Window		On/Off can be set.	
Bit Window		On/Off can be set.	
External Mask		On/Off can be set.	
Measurement			
Measurement types	Error Rate	0.0001E – 18 to 1.0000E – 00	
	Error Count	0 to 9999999, 1.0000E07 to 9.9999E17	
	Error Interval	0 to 9999999, 1.0000E07 to 9.9999E17	
	%Error Free Interval	0.0000 to 100.0000	
	Frequency	100.000 to 14,000.000 MHz (When MU181040B-002 is installed) 100.000 to 14,050.000 MHz (When MU181040B-003 is installed)	
	Frequency measurement accuracy	±1 ppm ±1 KHz(when the input CK signal and DCS board 10 MHz are calibrated correctly)	
	Clock Count	0 to 9999999, 1.0000E07 to 9.9999E17	
	Sync Loss Interval	0 to 9999999, 1.0000E07 to 9.9999E17	
	Clock Loss Interval	0 to 9999999, 1.0000E07 to 9.9999E17	
	CR Unlock Interval	0 to 9999999, 1.0000E07 to 9.9999E17	

Table 1.3.2-1 Specifications for MU181040B (Cont' d)

Item		Specifications	Remarks
Gating	Time, Clock Count, Error Count, and Block Count can be set.		
	Time	1 second to 99 days 23 hours 59 minute 59 seconds	
	Clock Count	1×10^n (n = 4 to 16)	
	Error Count	1×10^n (n = 4 to 16)	
	Block Count	1×10^n (n = 2 to 14)	
	Gating Cycle	Repeat, Single, and Untimed can be set.	
	Current	On/Off can be set.	
		Progressive/Immediate can be set.	
		100-ms/200-ms interval can be set.	
Auto Sync	On/Off can be set.		
	Synchronization threshold	INT, 1×10^{-n} (n = 2, 3, 4, 5, 6, 7, 8)	
Sync Control	Frame ON, Frame OFF, Quick, and Fast can be set. When Frame ON, Frame Length/Frame Mask/Frame Position are valid.		
	Frame length	4 to 64 bits (in 4-bit steps)	
	Frame mask	Available	
	Frame Position	1 to Pattern Length–Frame Length + 1,1 bit Step In the case of 2 Ch Combination: 1 to 1+2n, in 2-bit steps Maximum value of n = INT((Pattern Length – Frame Length)/2) In the case of 4 Ch Combination: 1 to 1+4n, in 4-bit steps Maximum value of n = INT((Pattern Length – Frame Length)/4)	
Error alarm conditions	Error detection mode	Total, Insertion/Omission, or Transition/Non Transition In the case of Combination: Transition/Non Transition cannot be selected	
	EI/EFI interval	1, 10, 100 ms, 1 s	
	Error performance	Available	
Capture function	Number of blocks	1, 2, 4, 8, 16, 32, 64, 128	
	Block length	1 Mbits to 128 Mbits 2 to 256 Mbits for 2 Ch Combination 4 to 512 Mbits for 4 Ch Combination	
Automatic measurement function	ISI analysis	Available. Number of blocks: 64 In the case of 2 Ch Combination, the number of blocks at the lowest layer is 128. In the case of 4 Ch Combination, the number of blocks at the lowest layer is 256.	
	Eye margin	Available	
	Eye diagram	Available	
	Q Analysis	Available	
	Bathtub	Available	

Table 1.3.2-1 Specifications for MU181040B (Cont'd)

Item		Specifications	Remarks
Burst measurement function	Source	Internal, External-Enable, External-Trigger	
	Burst Cycle	25,600 to 2,147,483,648 bits (in 128-bit steps) In the case of 2 Ch Combination: 51,200 to 4,294,967,296 bits, in 256-bit steps In the case of 4 Ch Combination: 102,400 to 8,589,934,592 bits, in 512-bit steps	
	Enable Period	Internal 12,800 to 2,147,483,136 bits, in 128-bit steps Other than Internal 12,800 to 2,147,483,520 bits, in 128-bit steps In the case of 2 Ch Combination: Internal 25,600 to 4,294,966,272 bits, in 256-bit steps Other than Internal 25,600 to 4,294,967,040 bits, in 256-bit steps In the case of 4 Ch Combination: Internal 51,200 to 8,589,932,544 bits, in 512-bit steps Other than Internal 51,200 to 8,589,934,080 bits, in 512-bit steps	
	Delay	Internal 0 to 2,147,483,648 bits, in 16-bit steps Other than Internal 0 to 2,147,483,584 bits, in 16-bit steps In the case of 2 Ch Combination: Internal 0 to 4,294,967,296 bits, in 32-bit steps Other than Internal 0 to 4,294,967,168 bits, in 32-bit steps In the case of 4 Ch Combination: Internal 0 to 8,589,934,592 bits, in 64-bit steps Other than Internal 0 to 8,589,934,336 bits, in 64-bit steps	

Table 1.3.2-1 Specifications for MU181040B (Cont'd)

Item		Specifications	Remarks
Data input	Number of inputs	2 (Data/XData Differential)	When MU181040B-002 is installed
	Input signal format	NRZ	
	Input condition	Single-ended, Differential 50 Ω, and Differential 100 Ω can be set. Data and XData can be set.	
	Input amplitude	0.1 to 2.0 Vp-p (when Single-ended is selected)	
	Threshold voltage	Independent, Tracking, and Alternate can be set. –3.500 to +3.300 V (in 1 mV steps) (Tracking/Independent) –3.000 to +3.000 V (in 1 mV steps) (Alternate)	
	Input sensitivity	10 mVp-p Typ. (at 10 or 12.5 Gbit/s, Single-ended input, PRBS: 2^{31}–1, mark ratio: 1/2, 20 to 30°C) 20 mVp-p Typ. (at 14 Gbit/s, 14.05Gbit/s*, Single-ended input, PRBS: 2^{31}–1, mark ratio: 1/2, 20 to 30°C)	* When MU181040B-003 is installed
	Phase margin	50 ps Typ. at 14 Gbit/s, 14.05Gbit/s* 60 ps Typ. at 12.5 Gbit/s 80 ps Typ. at 10 Gbit/s (at Single-ended input, PRBS: 2^{31}–1, mark ratio: 1/2)	
	Termination voltage	–2.50 to 3.50 V, 10 mV step(50 Ω/when Variable settng, load current <60 mA)	
	Termination	NECL, PCML, LVPECL, GND, Variable (–2.5 to +3.5 V)	
	Connector	K	
Clock input	Number of input	1 (Single-ended)	
	Input waveform	Rectangular wave (<0.5 GHz), Duty: 50%, Rectangular or sine wave (≥0.5 GHz), Duty: 50%	
	Input amplitude	0.25 to 1.5 Vp-p	
	Termination	50 Ω/GND, 50 Ω/Variable	
	Termination voltage	–2.50 to +3.50 V (in 10 mV steps) (50 Ω, when set to Variable, load current <60 mA)	
	Termination	NECL, PCML, LVPECL, GND, Variable (–2.5 to +3.5 V)	
	Connector	SMA	

Table 1.3.2-1 Specifications for MU181040B (Cont'd)

Item		Specifications	Remarks
AUX output	Number of outputs	1	
	Output Signal Selection	1/N Clock, Pattern Sync, Sync Gain, Error Output	
	Output signal	1/N: N=8,9,10…510,511	
	Pattern Sync		
	When PRBS, Data or Zero-sub is set	Position: 1 to {(Least common multiple of Pattern Length* and 64) -79}, in 16-bit steps. The maximum settable number is 68,719,476,657 In the case of 2 Ch Combination: 1 to {(Least common multiple of Pattern Length* and 128) -159}, in 32-bit steps. The maximum settable number is 137,438,953,313 In the case of 4 Ch Combination: 1 to {(Least common multiple of Pattern Length* and 256) -319}, in 64-bit steps. The maximum settable number is 274,877,906,625	
	When Mixed Data is set	Block No. setting: 1 to the Block No. specified for Mixed Data, in single steps	
		Row No. setting: 1 to the Row No. specified for Mixed Data, in single steps	
	When Sequence is set	Block No. setting: 1 to Block No. set for Sequence Pattern, in single steps	
		Position: 1 to {(Least common multiple of Pattern Length* and 64) -79}, in 16-bit steps.	
	Output level	0/–1 V H: –0.25 to 0.05 V L: –1.10 to –0.80 V	
	Impedance	50 Ω/GND	
	Connector	SMA	

* At Independent, when the pattern length is 127 bits or less, specify the length as an integer multiple so that it becomes 128 bits or more.
At 2 Ch Combination, when the pattern length is 255 bits or less, specify the length as an integer multiple so that it becomes 256 bits or more.
At 4 Ch Combination, when the pattern length is 511 bits or less, specify the length as an integer multiple so that it becomes 512 bits or more.

Table 1.3.2-1 Specifications for MU181040B (Cont'd)

Item		Specifications	Remarks
AUX input	Number of inputs	1	
	Input signal	In the case of Combination, input only to Master Module is enabled. Burst: External-Trigger (Data is enabled at rising edge detection) External-Enable (L: Data disabled, H: Data output) External Mask: (L: Measurement masked, H: Measurement) Capture External Trigger: (Start capture at rising edge detection)	
	Minimum pulse width	1/64 of Data rate	
	Input level	0/–1 V H: –0.25 to 0.05 V L: –1.10 to –0.80 V	
	Termination	50 Ω/GND	
	Connector	SMA	
Monitor output	Number of output	2 (Data monitor, XData monitor)	
	Insertion loss	–6 dB (+ 1 dB/–2.5 dB), at 7 GHz. (Data Input to Data Monitor Output, XData Input to XData Monitor Output)	
	Termination	AC/50 Ω	
	Connector	SMA	
Clock Recovery	Operating bit rate	100 Mbit/s 125 to 200 Mbit/s (steps: 125, 140.6,155.52, 156.3, 171.9, 187.5, 200 Mbit/s) 250 to 400 Mbit/s (steps: 250, 281.3, 312.5, 343.8, 375.0, 400 Mbit/s) 500 to 800 Mbit/s (steps: 500, 562.5, 622.08, 625.0, 687.5, 750.0, 800 Mbit/s) 1.0 to 1.6 Gbit/s (steps: 1.0, 1.0625, 1.125, 1.25, 1.375, 1.5, 1.6 Gbit/s) 2.0 to 3.2 Gbit/s (steps: 2.0, 2.125, 2.25, 2.48832, 2.5, 2.66606, 2.75, 3.0, 3.125, 3.2 Gbit/s) 4.25 Gbit/s, 4.9 to 6.25 Gbit/s (steps: 1 kbit/s), 9.8 to 12.5 Gbit/s (steps: 1 kbit/s)	When MU181040B-x20 is installed

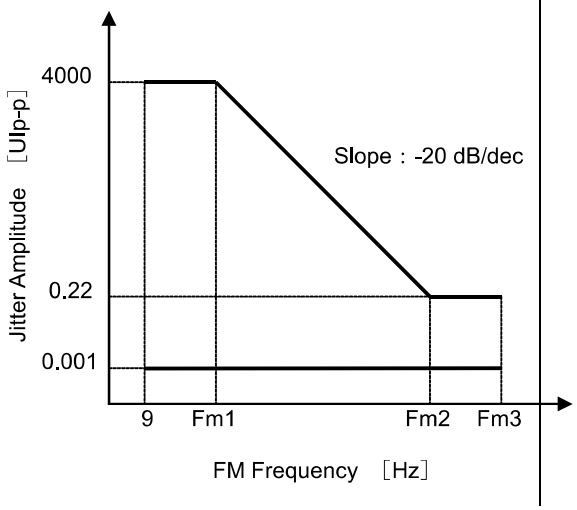
Table 1.3.2-1 Specifications for MU181040B (Cont'd)

Item		Specifications	Remarks
Clock Recovery (Cont'd)	Preset standards	10 GFC over FEC, 10 GbE over FEC, OTU2, G975 FEC, 10 GFC, 10 GbE, OC192/STM64, SATA 6 Gbit/s, PCI Express II, 4 GFC, XAUI, SATA 3 Gbit/s, OTU1, PCI Express I, OC48/STM16, 2 GFC, SATA 1.5 Gbit/s, GbE, 1 GFC, OC12/STM4, OC3/STM1	
	Input data	PRBS/Data/Zero-Sub/Mixed/Sequence NRZ (equivalent to mark ratio of 1/2)	
	Clock polarity switching	POS and NEG can be set. (when MU181040B-x30 is not installed)	
	Maximum length of successive 0	72 bits (Zero-Sub 15 stages, polarity: POS or NEG)	
	Lock range	±500 ppm (at 9.8 to 12.5 Gbit/s, 4.9 to 6.25 Gbit/s), ±100 ppm (at 4.25 Gbit/s)	
Recovered clock	Output count	1	
	Output amplitude	0.55 Vp-p ±0.15 V (at 12.5 GHz)	
	Duty	50 ±15%	
	Termination	50 Ω/GND	
	SSB phase noise	70 dBc/Hz Typ. at 10-kHz offset (2.488/4.25/9.95 GHz)	
	Jitter	<45 ps (p-p) at 2.488 Gbit/s <35 ps (p-p) at 4.25 Gbit/s <20 ps (p-p) at 9.953 Gbit/s (0.25 V (p-p) input PRBS31)	
	Jitter tolerance	2.488 Gbit/s Mask 15 UI (10 to 600 Hz modulation) 15 to 1.5 UI (600 Hz to 6 kHz modulation) 1.5 UI (6 to 100 kHz modulation) 1.5 to 0.15 UI (100 kHz to 1 MHz modulation) 0.15 UI (1 to 80 MHz modulation) 4.25 Gbit/s 0.67 UI Typ. (170 kHz modulation) 9.953 Gbit/s Mask 15.2 UI (10 to 2 kHz modulation) 15.2 to 1.7 UI (2 to 17.9 kHz modulation) 1.7 UI (17.9 to 400 kHz modulation) 1.7 to 0.17 UI (400 kHz to 4 MHz modulation) 0.17 UI (4 to 8 MHz modulation) 0.17 to 0.05 UI (8 to 27.2 MHz modulation) 0.05 UI (27.2 to 80 MHz modulation)	When MU181040B-x20 is installed
	Connector	SMA	

Table 1.3.2-1 Specifications for MU181040B (Cont'd)

Item		Specifications	Remarks
Clock phase variable	Phase variable range	In the case of 2 or 4 Ch Combination: –1000 to +1000 mUI, in 1-mUI step In the case of Channel Synchronization: –64,000 to +64,000 mUI, in 1-mUI steps	When MU181040B-x30 is installed
	Phase setting error	Typ. 20 mUIp-p mUI (After executing calibration)	
Auto Adjust Auto Search	Input Format	NRZ (when there is at least one transit bit for every 128 bits, the number of rising/falling edge ratio relative to Pattern Length is 1:5 or more, and the mark ratio is from 1/8 to 7/8)	
	Input Sensitivity	Typ. 200 mVp-p (25°C ±5°C)	

Table 1.3.2-1 Specifications for MU181040B (Cont'd)

<table>
<tr><th colspan="2">Item</th><th>Specifications</th><th>Remarks</th></tr>
<tr><td>Jitter</td><td>Jitter tolerance mask</td><td>


<table>
<tr><th>Fc ［GHz］</th><th>Fm1 ［Hz］</th><th>Fm2 ［Hz］</th><th>Fm3 ［Hz］</th></tr>
<tr><td>6.4 < Fc ≤ 14*</td><td>220</td><td>4 M</td><td>80 M</td></tr>
<tr><td>3.2 < Fc ≤ 6.4</td><td>110</td><td>2 M</td><td>40 M</td></tr>
<tr><td>1.6 < Fc ≤ 3.2</td><td>55</td><td>1 M</td><td>20 M</td></tr>
<tr><td>0.8 < Fc ≤ 1.6</td><td>27.5</td><td>500 k</td><td>10 M</td></tr>
<tr><td>0.1 ≤ Fc ≤ 0.8</td><td>13.75</td><td>250 k</td><td>5 M</td></tr>
</table>
* When installing the MU181020B-003, the upper frequency limit is 14.05 GHz can be used.

Measurement conditions
• "Internal" is selected for the modulation of
the MU181000A 12.5 GHz Synthesizer (with Option 001 installed) or
MU181000B 12.5 GHz 4 port Synthesizer
(with Option 001 installed) (hereinafter referred to as MU181000A/B).
• The MU181020B (with Option 002 installed) is used.
• Measurement pattern: PRBS $2^{31} - 1$
</td><td></td></tr>
</table>

Table 1.3.2-1 Specifications for MU181040B (Cont'd)

<table>
<tr><th colspan="2">Item</th><th>Specifications</th><th>Remarks</th></tr>
<tr><td>Jitter (continued)</td><td>Jitter tolerance (80 MHz or higher modulation)</td><td>
<table>
<tr><th>Fc [GHz]</th><th>FM Frequency [Hz]</th><th>Jitter Amplitude [Uip-p] (Max.)</th></tr>
<tr><td rowspan="2">11.3 < Fc ≤ 12.5</td><td>250 M to 1 G</td><td>0.1</td></tr>
<tr><td>80 to 250 M</td><td>0.22</td></tr>
<tr><td>8.5 < Fc ≤ 11.3</td><td>80 M to 1 G</td><td>0.22</td></tr>
<tr><td rowspan="2">8.0 < Fc ≤ 8.5</td><td>500 M to 1 G</td><td>0.1</td></tr>
<tr><td>80 to 500 M</td><td>0.22</td></tr>
<tr><td>4.0 < Fc ≤ 11.3</td><td>80 M to 1 G</td><td>0.22</td></tr>
<tr><td>2.4 < Fc ≤ 4.0</td><td>80 to 500 M</td><td>0.22</td></tr>
<tr><td>1.4 < Fc ≤ 2.4</td><td>80 to 100 M</td><td>0.22</td></tr>
</table>
Measurement conditions:
• "External" is selected for the modulation of the MU181000A/B (with Option 001 installed).
• The MU181020B (with Option 002 installed) is used.
In this event, Fc ≤ 1.4 GHz and Fm3 of the jitter tolerance mask above must be as follows:
<table>
<tr><th>Fc [GHz]</th><th>Fm3 [Hz]</th></tr>
<tr><td>0.65 < Fc ≤ 1.4</td><td>20 M</td></tr>
<tr><td>0.4 < Fc ≤ 0.65</td><td>10 M</td></tr>
</table>
• Measurement pattern: PRBS $2^{31} - 1$
• Use Recovered Clock at the clock recovery operation frequency (except 4.25 GHz) of the MU181040A (with Option x20 installed) (At other frequencies, use External input clock to assure the above performance).
• Ambient temperature: 25 ±5°C</td><td>When MU181040B-x20 is installed</td></tr>
</table>

Table 1.3.2-1 Specifications for MU181040B (Cont'd)

Item		Specifications	Remarks
Electrical size	Dimension	234 mm(W)×21 mm(H)×175 mm(D) (with Compact-PCI 1 slot but excluding protrusions)	
	Mass	2.5 kg max. (including options)	
Environmental performance	Operation temperature	+15 to +35°C (ambient temperature around equipment when installed in the mainframe)	
	Storage temperature	–20 to +60°C(Recommended storage temperature rang:+5 to +30°C)	