Discover What's Possible™

Anritsu

MP1763C/MP1764C/MP1764D

Pulse Pattern Generator/Error Detector

50 Mbit/s to 12.5 Gbit/s

- ***High-Quality, Low-Jitter, Low-Distortion Waveform Output***
- ***Evaluation of Transmission Modules, Buses, Backplanes using Differential/CDR Option***
- ***12.5 Gbit/s BERTS with Higher Performance and Lower Price***

High-Speed/Wide Band, High Quality Waveform and Advanced Functions

Today's demand for transfer of large amounts of data, such as video, over the internet, is resulting in expansion of high-speed transmission circuits and other infrastructure. In addition to the previously used STM-64/OC-192 (9.95328 Gbit/s) standards, we are also seeing use of 10.709225 Gbit/s (OTU-2), which includes FEC coding, as well as 3.125 Gbit/s x 4 and 10.3125 Gbit/s in 10 Gbit Ethernet. Furthermore, the Fibre Channel file transfer protocol at 4.25 Gbit/s is also coming into actual use.
As these new standards are settled upon, there is an urgent need to be able to support evaluation of devices and circuits at these higher bit rates.
Our MP1763C Pulse Pattern Generator and MP1764C/1764D Error Detector are a BERTS (Bit Error Rate Test Set) supporting evaluation and testing of transmission equipment, high-speed devices, optical modules, etc., at every stage from R&D through to manufacturing and production at speeds from 50 Mbit/s to 12.5 Gbit/s.

High-speed And Wide Band

One MP1763C/MP1764C can cover the band from STM-0/STS-1 to 10 Gbit Ethernet, STM-64/STS-192, OTU-2 and can be used with 4.25 Gbit/s Fibre Channel Systems.

Many Patterns

- 8 Mbit programmable pattern (corresponding to six frames of STM-64/STS192)
- PRBS patterns from $2^7 - 1$ to $2^{31} - 1$
- PRBS pattern with randomness and mark ratio variance for rigorous testing
- Alternating pattern
  The MP1763C alternately sends normal and alarm patterns to a device for response testing.
- Zero substitution pattern
  This feature is effective for testing the clock regeneration of a 3R repeater.

Location Changeable Pattern Synchronization Trigger

This feature makes it simple to monitor the waveform at any point in a long word pattern.

- High Q factor
  A high Q factor can be obtained by back to back connection (typical value at 10 Gbit/s, PRBS $2^{23} - 1$: 40 dB).

10 Gbit Ethernet I/O Interface Support

- **1/4 Differential Output (MP1763C-08 Option)**

This outputs differential data at a rate of 1/4 of the standard output (100 Mbit/s to 3.125 Gbit/s) as 4-bit parallel data. It can be used as a data signal for evaluating high-speed devices such as XAUI and SFI-4 P2 4 Lane devices used in 10 Gbit Ethernet and Fibre Channel, and for evaluating high-speed buses and backplanes such as PCI express.

- **Differential Input (MP1764C-02 Option)**

This can be used for evaluation by inputting a high-speed differential signal used by XAUI, SFI-4P2 4Lane devices, PCI Express, etc.

- **Clock Recovery Function (MP1764C-03 Option)**

The clock recovered from input data can be used as a trigger signal for error rate detection and waveform monitoring. Evaluation does not require an external clock, and when used jointly with differential input, high-speed differential devices can be evaluated without an external jig.
Bit rates from 62.5 Mbit/s to 11.1 Gbit/s are supported along with 4.25 Gbit/s used by Fibre Channel.

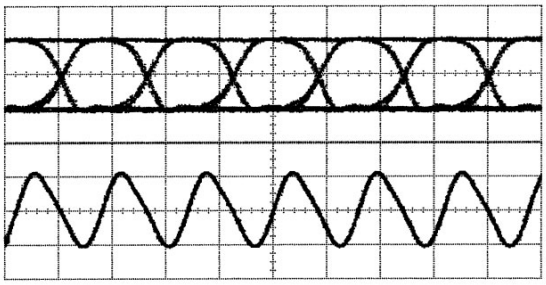
∗The MP1764D model ships with the MP1764C-02 (Differential input) and MP1764C-03 (Clock recovery) options installed.

Pulse Pattern Generator

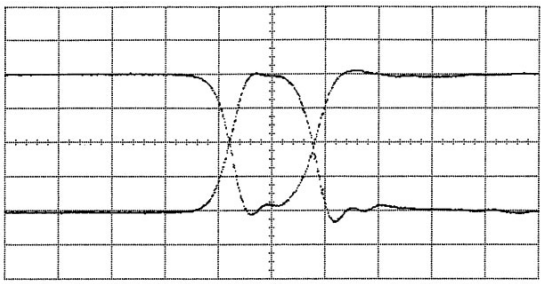
High-quality Waveform

- t_r/t_f (10% to 90%): 30 ps (typical)
- Jitter: 10 ps_{p-p} (typical)
- Back termination for low waveform distortion
- A pattern of isolated pulses which do not depend on mark ratios.

MP1763C output waveform



H: 50 ps/div, V: 1 V/div
DATA output of 12.5 GHz (top trace)
CLOCK 1 output (bottom trace)



H: 50 ps/div, V: 0.5 V/div
Isolated pattern (superimposition of 1/64 bits and 63/64 bits)

High Resolution Clock And Data Output

- Output amplitude: 0.25 to 2 Vp-p (2 mV steps)
- Output offset: –2 to +2 V (1 mV steps)
- Delay (clock): –500 to +500 ps (1 ps steps)
- DATA/DATA independently variable

Burst Signal Generation Using External Gate Signal

This feature is effective for optical fiber-loop testing, etc.

Parallel Output I/F (1/8, 1/4, 1/4 Differential)

- 1/8 parallel output is standard. 1/4 parallel output (Option 03) or 1/4 differential output (Option 08) can be selected exclusively.
- It can be used as a MUX device and a data generator for WDM transmission.
- The 1/4 differential option provides 4-bit parallel output of differential data for the 1/4 rate standard output (100 Mbit/s to 3.125 Gbit/s). Similarly, a 1/4 rate clock can be output as a differential. This can be used for performing detailed inspection of specifications and performance by use as a data signal for evaluation of high-speed devices such as XAUI and SFI-4 P2 4 Lane devices used in 10 Gbit Ethernet and Fibre Channel, and for evaluation of high-speed buses and backplanes such as PCI express.

Error Detector

High Input Sensitivity And Wide Phase Margin

- Input sensitivity: 50 mVp-p
  (typical value at 10 Gbit/s, PRBS $2^{23} - 1$)
- Phase margin: 70 ps or more
  (typical value at 10 Gbit/s, PRBS $2^{23} - 1$)

Eye Margin Measurement

The phase margin and threshold margin can be measured and displayed for any error rate.

Burst Measurement

- The burst data can be measured even for the PRBS and programmable patterns.
- High-speed synchronization gain is achieved by a quick synchronous method (typical sync. gain time at 10 Gbit/s, programmable pattern length of 2048 bits, sync. threshold at 10^{-2}: 850 ns).

Selectivity BER Measurement In Bit Units

The bit errors can be measured for any block of 32-bit segments or any bit.

Error Analysis Function (Option)

The pattern (256 bits in total) before and after a bit in which an error occurred can be displayed. Also, insertion and omission errors are displayed using different LED colors.

Differential Input Support (Option)

- This supports direct input of high-speed differential signals used by high-speed devices, buses and backplanes, such as XAUI, SFI-4 P2 4 Lane and PCI Express.
- Detailed evaluation is possible because independent thresholds can be set for inverted and non-inverted data

Clock Recovery Function (Option)

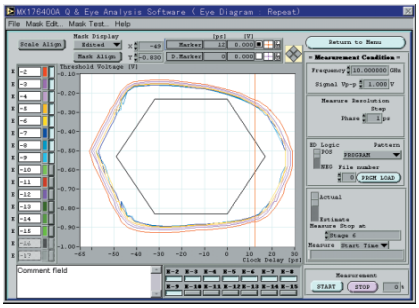
- The clock is recovered from the input data for use as a trigger signal at error rate detection and waveform monitoring. Evaluation does not require an external clock and the recovered clock can also be used as an external clock, depending on the setting.
- A wide range of bit rates from 62.5 Mbit/s to 11.1 Gbit/s is supported, along with the 4.25 Gbit/s rate used by Fibre Channel.
- When used in conjunction with differential input, it is also possible to evaluate the latest high-speed differential devices that do not use a clock without the need for an external jig.

Application Software

MX176400A Q/Eye Analysis Software

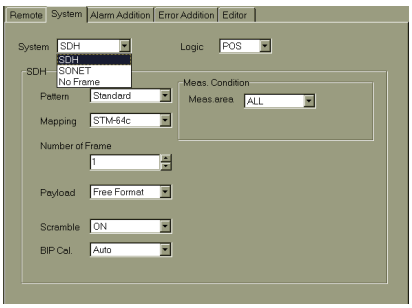
- Eye diagram and eye margin automatic measurement
- Displays a mask figure for the evaluation on the screen
- Q-factor (ITU-T G.976) automatic measurement

∗ Single input unsupported; use at differential signal input is not supported.



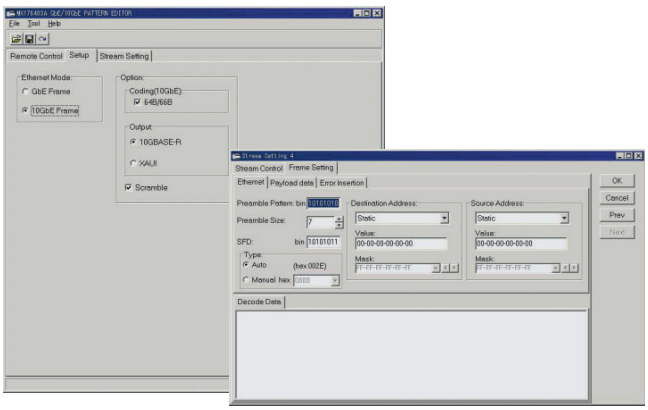
MX176401A SDH/SONET Pattern Editor

- Support OC-1 (STM-0) to OC-192c (STM-64c) mapping
- Alarm addition (OOF, LOF, MS-AIS, REI, RDI)
- BIP error addition (B1, B2, B3)
- Support “No frame” pattern

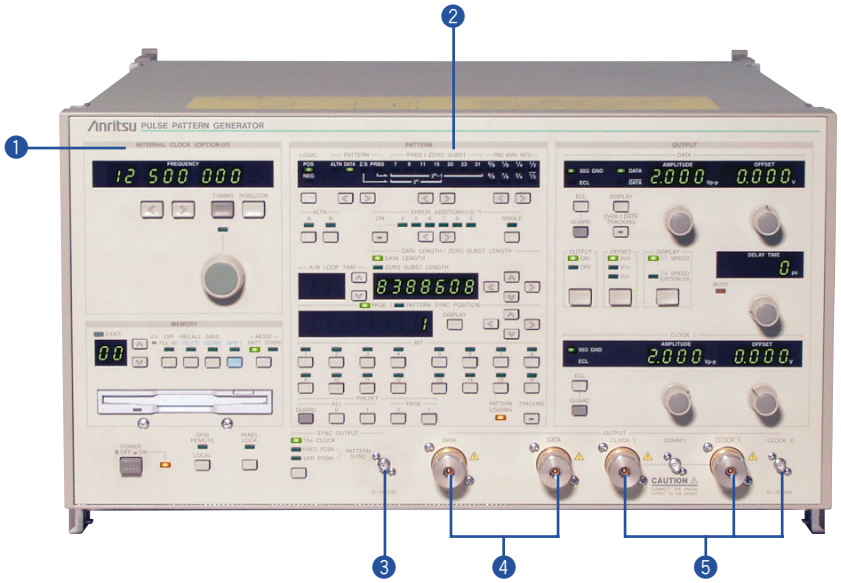


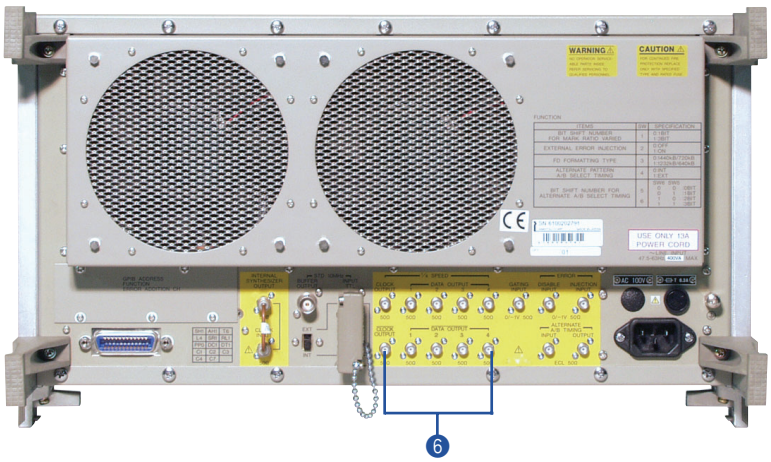
MX176403A GbE/10GbE Pattern Editing Software (At Order Acceptance)

- Supports Gbit Ethernet, 10 Gbit Ethernet (10GBASE-R, XAUI) frames
- 8B/10B, 64B/66B ON/OFF
- Header, Payload editing function
- CRC Auto-calculation
- Bit Error, FCS Error insertion function



MP1763C Pulse Pattern Generator





1 Internal Clock (Option 01)
Can be set in units of 1 kHz over the range from 50 MHz to 12.5 GHz

2 Programmable Patterns
- 8-Mbit programmable pattern (can set six STM-64 frames)
- 4-Mbit alternate pattern
- Zero substitution pattern
- PRBS pattern from $2^7 - 1$ to $2^{31} - 1$ selectable and its mark ratio can be varied.

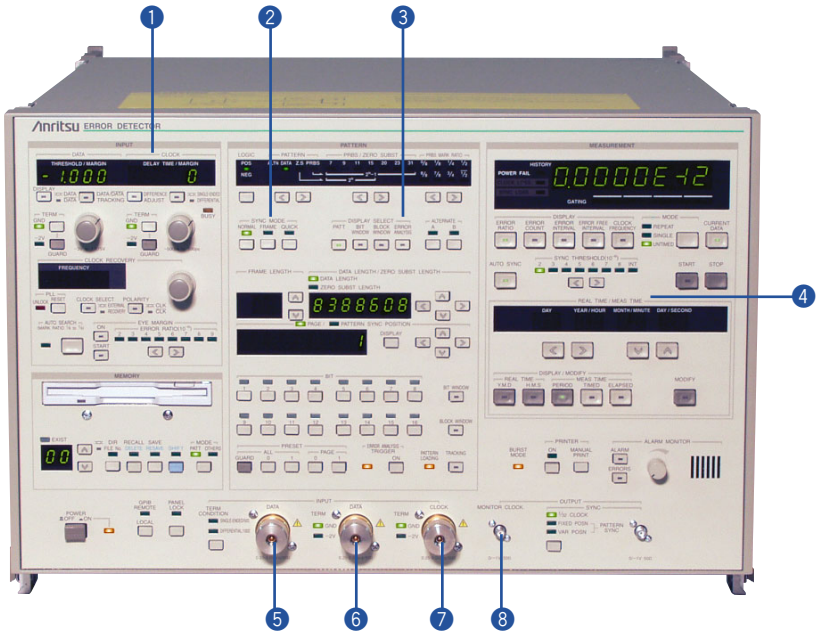
3 Synchronous Output
The 1/64 clock or pattern SYNC selectable.
The trigger position variable for the pattern SYNC

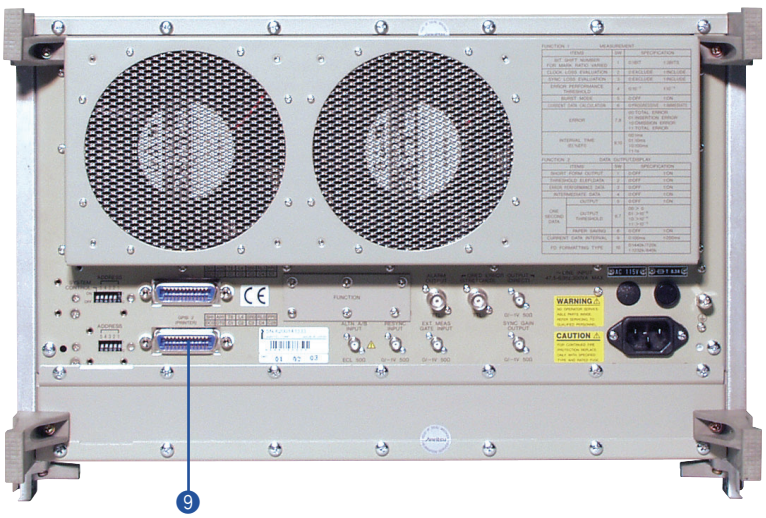
4 DATA Output
DATA/$\overline{\text{DATA}}$ complementary output with back termination

5 CLOCK Output
CLOCK 1/$\overline{\text{CLOCK 1}}$, CLOCK 2 (3 systems)
CLOCK 1/$\overline{\text{CLOCK 1}}$ with back termination

6 Parallel Output
Useful for testing an 8:1 MUX
(changeable to 1/4 speed output with option)
- 1/8 parallel output is standard. 1/4 parallel output (Option 03) or 1/4 differential output (Option 08) can be selected exclusively.
- It can be used as a data generator for evaluation of MUX devices, WDM transmission equipment, high-speed buses, back-planes, etc.

MP1764D Error Detector





1 Eye Margin Measurement
Displays the phase margin and threshold margin.

2 Synchronous Mode
High-speed sync. gain is achieved in frame and quick synchronous modes.

3 Error Analysis (Option 01)
The input pattern before and after a bit in which an error occurred can be checked.

4 Synchronous Threshold
The sync. gain and sync. loss conditions can be set.

5 Non-Inverted DATA Input
Has a high input sensitivity of 50 mVp-p (typical value).

6 Inverted DATA Input (Option 02)
At differential input, this uses inverted DATA input.

7 CLOCK Input
Input CLOCK determining phase evaluation of 0 or 1
Option 03 with CLOCK recovery function makes input unnecessary when inputting data with a supported bit rate.

8 Regenerated CLOCK Output (Option 03)
This outputs the CLOCK regenerated from DATA.

9 Two GPIB Connectors
One is used for an external printer.

Specifications

• MP1763C Pulse Pattern Generator

Operation frequency		0.05 to 12.5 GHz
Internal CLOCK (Option 01)		Frequency range: 0.05 to 12.5 GHz SSB phase noise: ≤–85 dBc/Hz (0.05 to 4 GHz), ≤–80 dBc/Hz (4 to 8 GHz), ≤–75 dBc/Hz (8 to 10 GHz), ≤–70 dBc/Hz (10 to 12.5 GHz) ∗At 10 kHz offset, 1 Hz bandwidth
External CLOCK input level		0.4 to 2.5 Vp-p
Pattern	Pseudorandom binary sequence pattern (PRBS)	Pattern: $2^n - 1$ (n: 7, 9, 11, 15, 20, 23, 31) Mark ratio: 1/2, 1/4, 1/8, 0/8 (1/2, 3/4, 7/8, 8/8 are possible with logic inversion) Bit shifts number for mark ratio varied: 1, 3 bits selectable
	DATA pattern	DATA length: 2 to 8388608 bits
	Alternate pattern	A/B pattern DATA length: 128 to 4194304 bits (128 bit steps); Loop time: A, B pattern (1 to 127, 1 steps)
	Zero substitution pattern	Zero bit length: 1 to (pattern length – 1) bits; Pattern: 2^n (n: 7, 9, 11, 15)
	Error addition	Error rate: 10^{-n} (n: 4, 5, 6, 7, 8, 9), and single error External error injection: Provided
DATA output	Number of outputs	2 (DATA/$\overline{\text{DATA}}$ independently)
	Amplitude	0.25 to 2 Vp-p, 2 mV steps
	Offset voltage	V_{OH}: –2 to +2 V, 1 mV steps Display: V_{OH}, V_{TH} or V_{OL} selectable
	Rise/fall time	Typical 30 ps (10% to 90% of amplitude)
	Pattern jitter	≤20 psp-p, typical 10 psp-p
	Waveform distortion (0-peak)	≤15% or ≤150 mV whichever is greater
	Gating input	Provided
	Load impedance	50 Ω (with back termination)
	Connector	APC-3.5
	DATA/$\overline{\text{DATA}}$ tracking	$\overline{\text{DATA}}$ amplitude and offset voltage can be set to the same values as for DATA.
	Cross point adjustment function	The cross point of DATA/$\overline{\text{DATA}}$ outputs can be adjusted at semifixed resistor of side.
CLOCK output	Number of outputs	3 (CLOCK 1/$\overline{\text{CLOCK 1}}$, CLOCK 2)
	Amplitude	CLOCK 1/$\overline{\text{CLOCK 1}}$: 0.25 to 2 Vp-p (2 mV steps) CLOCK 2: 1 Vp-p
	Offset voltage	CLOCK 1/$\overline{\text{CLOCK 1}}$: V_{OH} –2 to +2 V (1 mV steps) CLOCK 2: V_{OH} 0 V fixed
	Rise/fall time	Typical 30 ps (10% to 90% of amplitude)
	Load impedance	50 Ω (CLOCK 1/$\overline{\text{CLOCK 1}}$: with back termination)
	Connector	CLOCK 1/$\overline{\text{CLOCK 1}}$: APC-3.5, CLOCK 2: SMA
	Delay	±500 ps (1 ps steps)
1/8 DATA and CLOCK output	Number of outputs	DATA 8, CLOCK 1
	Output level	ECL
	Connector	SMA
1/4 DATA and CLOCK output (Option 03)[*1]	Number of outputs	DATA: 4, CLOCK: 1
	Amplitude	0.5 to 2 Vp-p (2 mV steps)
	Offset voltage	V_{OH}: –1.5 to +1.5 V (1 mV steps)
	Connector	SMA
1/4 Differential DATA, CLOCK output (Option 08)[*1]	Operation bit rate	1/4 DATA/$\overline{\text{DATA}}$: 100 Mbit/s to 3.125 Gbit/s
	Number of outputs	1/4 DATA/$\overline{\text{DATA}}$ differential 4 system. 1/4 CLOCK/$\overline{\text{CLOCK}}$ differential 1 system
	Amplitude	0.5 to 2.0 Vp-p (2 mV steps), 1/4 DATA/$\overline{\text{DATA}}$: All channels same settings
	Offset voltage	1/4 DATA/$\overline{\text{DATA}}$: –1.0 to +2.5 V (V_{OH}) (1 mV steps, PRBS 50 Ω/GND termination) All channels same settings 1/4 CLOCK/$\overline{\text{CLOCK}}$: –1.5 to +1.5 V (V_{OH}) (1 mV steps, PRBS 50 Ω/GND termination)
	Connector	SMA
Sync. signal output	Number of outputs	1 (1/64 CLOCK, fixed position pattern, or variable position pattern selectable)
	Output level	0/–1 V
	Connector	SMA
Parameter memory		Media: 3.5 inch FD (2HD, 2DD), Format: MS-DOS (Rev. 3.1)[*2], Content: Pattern or other parameters
Operating temperature range		0˚ to +50˚C
Dimensions and mass		426 (W) x 221 (H) x 450 (D) mm, ≤33 kg
Power		≤400 VA
EMC		EN61326: 1997/A2: 2001 (Class A), EN61000-3-2: 2000 (Class A), EN61326: 1997/A2: 2001 (Annex A)
LVD		EN61010-1: 2001 (Pollution Degree 2)

∗1: Select one type from three items
- 1/8 DATA and 1/8 CLOCK output
- 1/4 DATA and 1/4 CLOCK output (Option 03)
- 1/4 Differential DATA and 1/4 Differential CLOCK output (Option 08)

∗2: MS-DOS is a registered trademark of Microsoft Corporation.

• MP1764C/MP1764D Error Detector

Operation frequency		0.05 to 12.5 GHz
DATA/$\overline{\text{DATA}}$ input (MP1764D Option 02)	Input waveform	NRZ
	Input amplitude	0.25 to 2.0 Vp-p
	Threshold voltage variable range	–3.000 to +1.875 Vp-p (1 mV steps)
	Phase margin	≥70 ps (typical value at 10 Gbit/s, PRBS 2^{23} – 1, at single ended input amplitude of 1 Vp-p)
	Input sensitivity	50 mVp-p (typical value at 10 Gbit/s and PRBS 2^{23} – 1)
	Termination	Connected to GND or –2 V via a 50 Ω termination
	Connector	APC-3.5
CLOCK input	Input waveform	Rectangular wave (<0.5 GHz), rectangular or sine wave (≥0.5 GHz), duty factor: 50%
	Input voltage	0.25 to 2.0 Vp-p
	Input delay variable range	±500 ps (1 ps steps)
	Polarity inversion	CLOCK/$\overline{\text{CLOCK}}$ inversion possible
	Termination	Connected to GND or –2 V via a 50 Ω termination
	Connector	APC-3.5
CLOCK regeneration function (MP1764D Option 03)	Operation bit rate	62.5 to 100 Mbit/s, 125 to 200 Mbit/s, 250 to 400 Mbit/s, 500 to 800 Mbit/s, 1,000 to 1,600 Mbit/s, 2,000 to 3,200 Mbit/s, 4,250 Mbit/s ±50 ppm, 9,900 to 11,100 Mbit/s
	CLOCK selection	Internal/External
	Continuous 0 s tolerance (withstand)	72 bit min.
	Regenerated CLOCK output	Output level: 1.0 ±0.25 V (AC coupling)
Auto search function		Provided
Receive pattern	Pseudorandom binary sequence pattern (PRBS)	Pattern: 2^n – 1 (n: 7, 9, 11, 15, 20, 23, 31) Mark ratio: 1/2, 1/4, 1/8, 0/8 ($\overline{1/2}$, 3/4, 7/8, 8/8 are possible with logic inversion.) Number of AND bit shift at mark ratio setting: 1, 3 bits (selectable by using DIP switch on rear panel)
	DATA pattern	DATA length: 2 to 8388608 bits
	Alternate pattern	A/B pattern word length: 128 to 4194304 bits (128 bits steps), Number of loops: Controlled using external signal
	Zero substitution pattern	Zero bit length: 1 to (pattern length –1) bits, Pattern length: 2^n (n: 7, 9, 11, 15)
Synchronous mode		Normal, frame, quick
Synchronous threshold		Preset value or 10^{-n} (n: 2, 3, 4, 5, 6, 7, 8)
Error detection mode		Omission insertion, total (selectable with DIP switch on rear panel)
Measure-ment item	Error rate	0.0000 x 10^{-16} to 1.0000 x 10^{-0}
	Number of errors	0 to 9.9999 x 10^{16}
	Error interval (asynchronous)	0 to 9999999 (interval: 1 ms, 10 ms, 100 ms, 1 s)
	Error free interval (EFI)	0.0000% to 100.0000%
	CLOCK frequency	0.05 to 12.5 GHz, (resolution: 1 kHz, accuracy: 10 ppm ±1 kHz)
Eye margin measurement function		Provided
Error performance DATA calculation function		Provided
Measurement CH mask		1 to 32 ch (settable independently)
Block window		Error for any block of 32-bit segments can be measured.
Error analysis (option 01)		Pattern (256 bits in total) before and after bit in which error occurred is stored.
Auxiliary output	Error output (direct)	1/128 OR error, Output level: 0/–1 V, Connector: SMA
	Error output (stretched)	Pulse width: 350 ns (typical), Output level: TTL, Connector: BNC
	Alarm output (CLOCK loss, sync. loss)	Output level: TTL Connector: BNC
	Sync. gain output	Output level: 0/–1 V; Connector: SMA
Auxiliary input	External mask input	Input level: 0/–1 V; Connector: SMA
	Resync. input	Input level: 0/–1 V; Connector: SMA
	Alternate A/B switching input	Input level: ECL; Connector: SMA
Sync. signal output	Number of outputs	1 (1/32 CLOCK, fixed position pattern, or variable position pattern selectable)
	Output level	0/–1 V
	Connector	SMA
Parameter memory		Media: 3.5 inch FD (2HD, 2DD), Format: MS-DOS (Rev. 3.1)*1, Content: Pattern or other parameters
Operating temperature range		0˚ to +50˚C
Dimensions and mass		426 (W) x 221.5 (H) x 450 (D) mm, ≤30 kg (except Option 02, 03) 426 (W) x 266 (H) x 450 (D) mm, ≤35 kg (Option 02, 03)
Power		≤300 VA
EMC		EN61326: 1997/A2: 2001 (Class A), EN61000-3-2: 2000 (Class A), EN61326: 1997/A2: 2001 (Annex A)
LVD		EN61010-1: 2001 (Pollution Degree 2)

*1: MS-DOS is a registered trade mark of Microsoft Corporation.

Ordering Information

Please specify model/order number, name and quantity when ordering.

Model/Order No.	Name
	Main frame
MP1763C	Pulse Pattern Generator (50 Mbit/s to 12.5 Gbit/s)
	Standard accessories
J0500A	Semi-rigid cable (SMA-P · UT-141 · SMA-P), 0.5 m: 2 pcs
J0672F	Semi-rigid cable (SMA-P · UT-85 · SMA-P), 10 cm: 1 pc
J0693A	SMA cable (HRM202B-3D2W-HRM202B), 1 m: 1 pc
J0496	APC-3.5 J-J connector: 4 pcs
J0008	GPIB cable, 2 m: 1 pc
J0491	Power cord: 1 pc
Z0168	3.5-inch floppy disk (MF2HD-3.5MF): 2 pcs
Z0481	12.5G/3.2G BERTS application software demo: 1 pc
Z0306A	Wrist strap: 1 pc
F0014	Fuse, 6.3 A (T6.3A250V): 1 pc
B0021	Protective cover (for 1MW · 5U): 1 pc
W1848AE	MP1763C operation manual: 1 copy
W1849AE	MP1763C GPIB operation manual: 1 copy
	Option
MP1763C-01	12.5 GHz Synthesizer (50 MHz to 12.5 GHz)
J0672D	Semi-rigid cable (SMA-P · UT-85 · SMA-P), 7 cm
MP1763C-03	1/4 speed output
MP1763C-08	1/4 Differential Data Output Function (100 Mbit/s to 3.125 Gbit/s)
W2339AE	MP1763C-08 operation manual
W2340AE	MP1763C-08 GPIB operation manual
	Main frame
MP1764C	Error Detector (50 Mbit/s to 12.5 Gbit/s)
MP1764D	Error Detector (50 Mbit/s to 12.5 Gbit/s)
	Standard accessories
J0500A	Semi-rigid cable (SMA-P · UT-141 · SMA-P), 0.5 m: 2 pcs (MP1764C) 4 pcs (MP1764D)
J0693A	SMA cable (HRM202B-3D2W-HRM202B), 1 m: 3 pcs
J0496	APC-3.5 J-J connector: 2 pcs (MP1764C) 3 pcs (MP1764D)
J0008	GPIB cable, 2 m: 2 pcs
J0776D	BNC cable (BNC-P · 3W · 3D · 2W · BNC-P · 3W), 2 m: 2 pcs

Model/Order No.	Name
J0491	Power cord (13 A): 1 pc
Z0168	3.5-inch floppy disk (MF2HD-3.5MF): 2 pcs
F0014	Fuse, 6.3 A: 1 pc
Z0306A	Wrist strap: 1 pc
B0021*1	Protective cover (for 1MW · 5U): 1 pc
B0022*2	Front cover: 1 pc
W1850AE	MP1764C operation manual: 1 copy
W1851AE	MP1764C GPIB operation manual: 1 copy
W2341AE	MP1764D operation manual: 1 copy
W2342AE	MP1764D GPIB operation manual: 1 copy
	Option
MP1764C-01	Error Analysis
MP1764C-02	Differential Data Input Function
MP1764C-03	Clock Recovery Function
MP1764D-01	Error Analysis
W2373AE	MP1764C-02,03 operation manual
W2374AE	MP1764C-02,03 GPIB Programming operation manual
	Application Software
MX176400A	Q/Eye Analysis Software
MX176401A	SDH/SONET Pattern Editor
MX176403A	GbE/10GbE Pattern Editor
	Optional accessories
J0500B	Semi-rigid cable (SMA-P · SX-36 · SMA-P), 1 m
J0322A	Coaxial cable (SUC0FLEX104, 11SMA-11SMA), 0.5 m
J0322B	Coaxial cable (SUC0FLEX104, 11SMA-11SMA), 1 m
J0007	408JE-104 GPIB cable, 1 m
Z0054	3.5-inch floppy disk (MF2DD-3.5MF)
MB24B	Portable Test Rack (rating current of power cord and plug: 20 A)
B0413A	Carrying case
B0163	Portable Quilting
B0044	Rack mount kit (for 1MW · 5U panel)
Z0416	3.5-inch head cleaning disk
J0498	Coaxial code, 0.5 m
J0499	Coaxial code, 1 m
J1141	50 Ω Terminator

*1: For MP1764C

*2: For MP1764C-02,03 and MP1764D

Anritsu

Specifications are subject to change without notice.

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040602

Catalog No. MP1763/1764-E-A-1-(4.00) Printed in Japan 2004-6 ddc