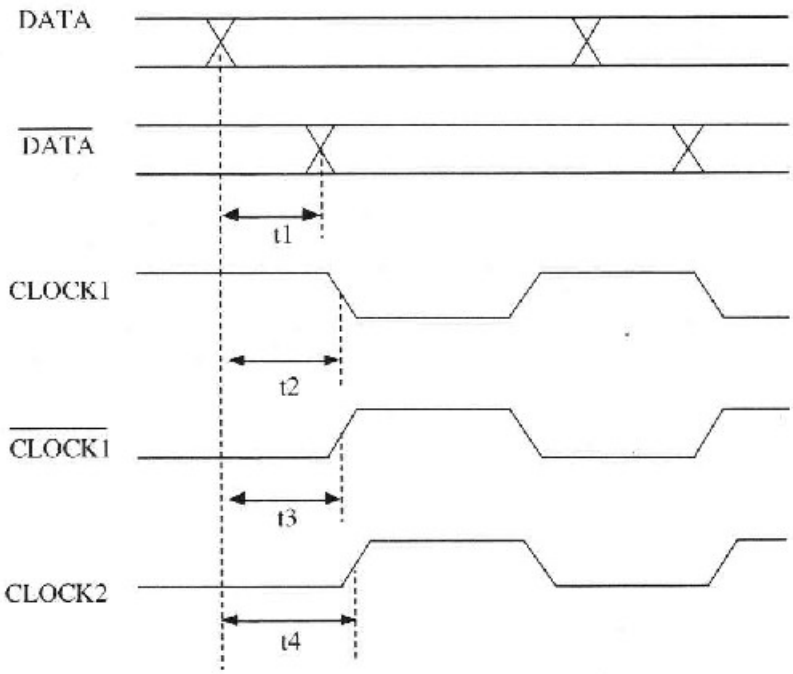
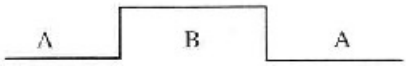
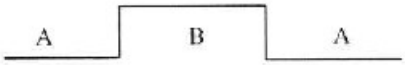
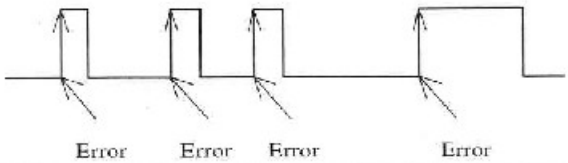
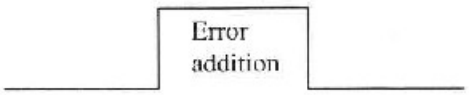
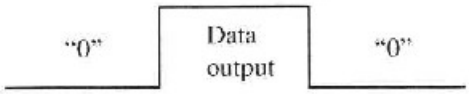
1.2 Specifications

Operation frequency range	Internal Clock (OPTION 01)		0.05 to 12.5 GHz
	External Clock		0.05 to 12.5 GHz
Pattern generation	PRBS	Pattern length	2^N-1 (N=7,9,11,15,20,23,31)
		Mark ratio	1/2,1/4,1/8,0/8 (1/2,3/4,7/8,8/8 also possible by logic inversion)
		Number of "AND bit" shifts when setting mark ratio	1 bit or 3 bits (Selectable using rear panel DIP switch)
	Zero substitution		Continuous 0 pattern can be inserted up to pattern length -1. Patterns: 2^7, 2^9, 2^{11}, 2^{15}
	DATA	DATA length	2 to 8388608 bits 2 to 65536 : Step 1 bit 65536 to 131072 : Step 2 bits 131072 to 262144 : Step 4 bits 262144 to 524288 : Step 8 bits 524288 to 1048576 : Step 16 bits 1048576 to 2097152 : Step 32 bits 2097152 to 4194304 : Step 64 bits 4194304 to 8388608 : Step 128 bits
		Edit function	All 0 / All 1 / Page 0 / Page 1
	Alternate pattern		Number of patterns A and B to be output can be specified. Patterns A and B must be the same length.
		Output control	Internal/external switchable
		A/B switching	A/B each 1 to 127 times/step 1
		DATA length	128 to 4194304 bits/step 128 bits
		Edit function	All 0 / All 1 / page 0 / page 1
	Logic inversion		Positive / Negative switching possible [PRBS]  [PRGM] 

Pattern generation	Error insertion	Internal	Error ratio	1×10^{-n} or single (n = 4 , 5, 6, 7 , 8 , 9)
			Insertion position	Insertion possible at any one of 32 channels (Rear panel swith)
		External	Eror injection	Error insertion by rising edge of external signal input
			Insertion position	Insertion possible at any one of 32 channels (Rear panel switch)
			DISABLE function	Error insertion when external signal input level is "H"
			Error ratio	1×10^{-n} or single (n = 4 , 5, 6, 7 , 8 , 9)
			Insertion position	Insertion possible at any one of 32 channels (Rear panel switch)
	Gating input			DATA is set to "0" while external signal input level is "L".
External Clock Input	Frequency range			0.05 to 12.5 GHz
	Input level			0.4 to 2.5 Vp-p
	Input waveform			0.05 to 0.5 GHz : Square wave only > 0.5 GHz: Sine wave or square wave (duty 50 %)
	Input impedance			50 Ω
	Connector			SMA
Clock output	Number of outputs			CLOCK1/$\overline{\text{CLOCK1}}$, CLOCK2 3 systems
	CLOCK1 / $\overline{\text{CLOCK1}}$	Delay range		±500 ps/1 ps step
		Amplitude		0.25 to 2.0 Vp-p/Step 2 mV Setting error: ±15% (1.5 to 2.0 Vp-p), ±25 % (0.5 to 1.5 Vp-p), ±100 mV(0.25 to 0.5 Vp-p)
		Offset		-2.0 to 2.0 V (VOH) /Step 1 mV Setting error: ± 15 % or ± 15 % of Amplitude, and ±100 mV, whichever is larger
		Rise/fall times (10%–90%)		≧ 8 GHz 1.5 to 2 Vp-p 35 ps or less < 8 GHz 1.5 to 2 Vp-p 50 ps or less ≧ 8 GHz 1.0 to 1.5 Vp-p 40 ps or less < 8 GHz 1.0 to 1.5 Vp-p 55 ps or less ≧ 8 GHz 0.25 to 1.0 Vp-p 45 ps or less < 8 GHz 0.25 to 1.0 Vp-p 60 ps or less
		Waveform distortion		15 % or less or 150 mV, whichever is larger
		Duty ratio adjust function		Duty ratio can be adjusted by semifixed variable resistor
		Load impedance		50 Ω (with back termination)
		Termination		50 Ω/GND, 50 Ω/–2 V
		Connector		APC-3.5
	CLOCK2	Output level		VOH : 0 ± 200 mV Amplitude: 1 Vp-p ±35 %
		Load impedance		50 Ω (without back termination)
		Connector		SMA

DATA output	Output waveform	NRZ
	Number of outputs	DATA, $\overline{\text{DATA}}$ 2 systems independence
	Amplitude	0.25 to 2.0 Vp-p/Step 2 mV Setting error: ±15 % or ±100 mV, whichever is larger
	Offset voltage	–2.0 to 2.0 V (V_{OH}) /Step 1 mV Setting error: ±15 % or +15 % of Amplitude , and ±100 mV, whichever is larger
	DATA/$\overline{\text{DATA}}$ Tracking	Amplitude and offset of DATA and $\overline{\text{DATA}}$ can be set to the same value.
	Rise / fall time	≥5 GHz, amplitude 1 to 2 Vp-p 35 ps or less (10-90 %) ≧5 GHz, amplitude 0.5 to 1 Vp-p 40 ps or less (10-90 %) ≥5 GHz, amplitude 0.25 to 0.5 Vp-p 45 ps or less (10-90 %) < 5 GHz 45 ps or less (10-90 %)
	Pattern jitter	20 ps or less (p-p)
	Waveform distortion	7 % or less, or 100 mV or less, whichever is larger.
	Termination	50 Ω/GND, 50 Ω/–2 V
	Load impedance	50 Ω (with back termination)
	Connector	APC-3.5
Output phase		|t1| ≦30 ps |t2| ≦30 ps |t3| ≦30 ps |t4| ≦30 ps CLOCK1/$\overline{\text{CLOCK1}}$ delay set to 0 ps

1/8 output	Number of output	8 data outputs, 1 clock output
	Data polarity	Same as 1/1 DATA
	Output level	ECL (H: –0.9 ±0.25 V, L: –1.75 ±0.25 V)
	Rise / fall time	300 ps or less (20-80 %)
	Pattern jitter	100 ps or less (p-p)
	Waveform distortion	15 % or less
	Skew	150 ps or less (relative to falling edge of 1/8 clock)
	Output bit rate	1/8 of fundamental frequency
	Load impedance	50 Ω
	Connector	SMA
Sync. output		Switching of 1/64 CLOCK, Fixed position pattern sync, and Variable position pattern sync.
	Output level	V_{OH}: 0±200 mV Amplitude: 1 Vp-p±20 %
	Load impedance	50 Ω
	Connector	SMA
Alternate pattern A/B switching input		ALTN patterns A/B switching controlled by external signal 
	Minimum pulse width	$\frac{1}{\text{Fundamental frequency}}$ × Data length
	Input level	ECL (H: –0.9 ±0.2 V, L: –1.75 ±0.2 V)
	Input impedance	50 Ω
	Connector	SMA
Alternate pattern A/B switching output		ALTN patterns A/B switching signal output 
	Output level	ECL (H: –0.9 ±0.2 V, L: –1.75 ±0.2 V)
	Output impedance	50 Ω
	Connector	SMA
Error injection input		Error inserted at rising edge by external signal 
	Minimum pulse width	$\frac{1}{\text{Fundamental frequency}}$ x 128
	Input level	0/–1 V
	Input impedance	50 Ω
	Connector	SMA

Error Disable input		Error ON/OFF controlled by external input signal  Error rate can be selected over this range
	Input level	0/-1 V
	Input impedance	50 Ω
	Connector	SMA
External Gating input		Output data control by external signal 
	Minimum pulse width	$\frac{1}{\text{Fundamental frequency}} \times 128$
	Input level	0/-1 V
	Input impedance	50 Ω
	Connector	SMA
Parameter memory	Medium	3.5 inch FD, 2HD, 2DD by 3 mode support
	Format	MS-DOS format (IBM-PC/NEC-PC selectable by rear panel DIP switch)
	Stored data	Programmable pattern/others
	Mode switching	Format, save, recall, resave, delete, search
Display	Display switching	V_{OH}, V_{TH}, V_{OL} switchable
	Panel lock	Disables all keys other than power switch.
External control	GPIB interface for one system	
GPIB	GPIB connector for external control	
Initialization	Inirialized by Local + Power on	
Operating temperature range	0 to 50 ℃	
Insulation resistance	2 MΩ or more at 500 V	
Dielectric strength	1.5 kV, for 1 minute	
Power requirement	100 V system: 85 to 132 V Frequency 47.5 to 63 Hz 400 VA or less	200 V system: 170 to 264 V
Dimensions & weight	221.5H×426W×451D, 33 kg or less	

Option-01	Name	Internal synthesizer
	Frequency range	0.05 to 12.5 GHz
	Output level	0.5 to 2.3 Vp-p
	Resolution	1 kHz/1 MHz (switchable)
	Frequency accuracy	1ppm (* When synchronized with external signal, accuracy is determined by external signal.)
	Reference signal	10 MHz (internal/external switchable)
	Signal purity	SSB phase noise (10 kHz offset, bandwidth 1 Hz) 0.05 ≦ Freq. < 2.0 GHz –90 dBc 2.0 ≦ Freq. < 4.0 GHz –85 dBc 4.0 ≦ Freq. < 8.0 GHz –80 dBc 8.0 ≦ Freq. <10.0 GHz –75 dBc 10.0 ≦ Freq. ≦12.5 GHz –70 dBc
	Spurious radiation	At clock output terminal Nonharmonic –70 dBc or less (off carrier 10 kHz or more) Power supply –40 dBc or less
	Load impedance	50 Ω
	Connector	SMA
Option-03*	Name	1/4 SPEED OUTPUT
	Number of output	4 data outputs, 1 clock output
	Output bit rate	1/4 of fundamental frequency
	Data polarity	Same as 1/1 DATA
	Termination	50 Ω/GND, 50 Ω/–2 V
	Amplitude	0.5 to 2.0 Vp-p/Step 2 mV Setting error: ±15% or ±100 mV, whichever is larger
	Offset voltage	–1.5 to +1.5 V (V_{OH})/Step 1 mV Setting error: ±15 % or ±15 % of Amplitude, and ±100 mV, whichever is larger
	Rise/fall time	150 ps or less (20-80 %)
	Pattern jitter	100 ps or less (p-p)
	Waveform distortion	15 % or less
	Skew	The 1/4 data cross point is within ±100 ps relative to the falling edge of the 1/4 clock.
	Output impedance	50 Ω
	Connector	SMA

* When OPTION 03 is installed, there is no 1/8 output.