Digital Delay/Pulse Generator

DG645 — Digital delay and pulse generator (4 or 8 channels)

DG645 Digital Delay/Pulse Generator

- ***4 pulse, 8 delay outputs (opt.)***
- ***<25 ps rms jitter***
- ***Trigger rates to 10 MHz***
- ***Precision rate generator***
- ***Fast transition times***
- ***Ovenized crystal or Rb timebase (opt.)***
- ***Ethernet, GPIB and RS-232 interfaces***
- ***DG645 ... $3995** (U.S. list)*

The DG645 is a versatile digital delay/pulse generator that provides precisely defined pulses at repetition rates up to 10 MHz. The instrument offers several improvements over older designs — lower jitter, higher accuracy, faster trigger rates, and more outputs. The DG645 also has Ethernet, GPIB and RS-232 interfaces for computer or network control of the instrument.

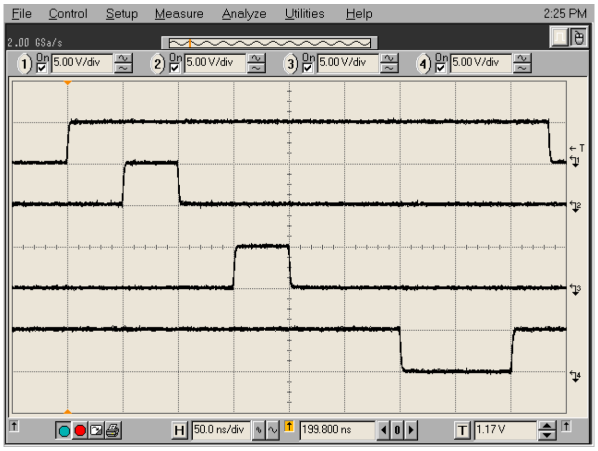
Delay Generator Timing

All digital delay generators measure time intervals by counting cycles of a fast clock (typically 100 MHz). Most digital delay generators also have short programmable analog delays to achieve time intervals with finer resolution than the clock period. Unfortunately, one clock cycle of timing indeterminacy (typically 10 ns) can occur if the trigger is not in phase with the clock.

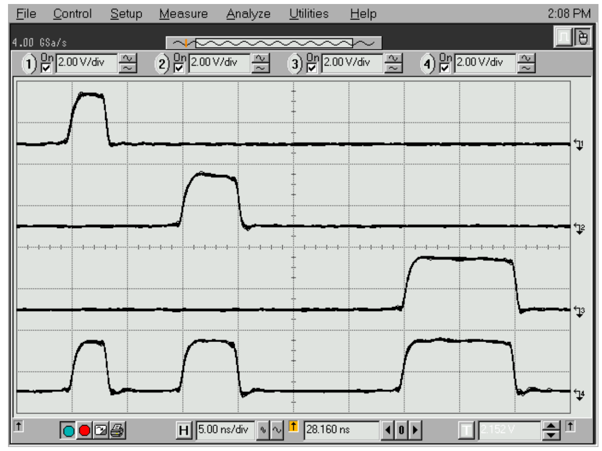
The DG645 eliminates timing indeterminacy by measuring the timing of triggers with respect to the internal clock and compensating the analog delays. This approach reduces the jitter by about 100× and allows the internal rate generator to operate at any rate — not just a sub-multiple of the clock frequency.

Triggering

The DG645 has many trigger modes. An internal rate generator, with less than 100 ps period jitter, may be set from



Front-panel outputs (50 ns/div)



Combinatorial outputs showing 3 ns, 5 ns and 10 ns pulses with 1 ns transition times (5 ns/div)

100 µHz to 10 MHz with 1 µHz resolution. An external trigger input, with adjustable threshold and slope, can trigger a timing cycle, a burst of cycles, or a single shot. A single shot can be triggered with a key press. A line trigger operates synchronously with the AC mains. A rear-panel trigger inhibit input can disable the trigger or any of the pulse outputs during a timing cycle.

Front-Panel Outputs

There are five front-panel outputs: T_0, AB, CD, EF and GH. The T_0 output is asserted for the duration of the timing cycle. The leading edge of T_0 is the zero time reference. The programmed delays (A, B, C, D, E, F, G and H) are set from 0 s to 2000 s, with 5 ps resolution, to control the timing of the leading and trailing edges of the four pulse outputs.

Each front-panel output can drive a 50 Ω load and has a 50 Ω source impedance. Output amplitudes can be set from 0.5 to 5.0 V, and output offsets can range over ±2 VDC to source virtually any logic level (NIM, ECL, PECL, CMOS, etc.). Output transition times are less than 2 ns at any output amplitude.

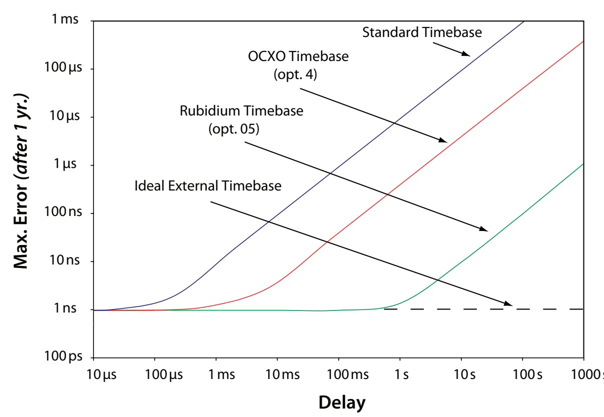
Rear-Panel Outputs

Optional rear-panel outputs are available to support diverse applications. Option 1 provides a T_0 output and eight programmed delays (A, B, C, D, E, F, G and H) at 5 V logic levels, with transition times less than 1 ns. Option 2 provides these same outputs but as 30 V, 100 ns pulses with less than 5 ns transition times for timing distribution in high noise environments. Option 3 provides eight combinatorial outputs which deliver one to four pulses at 5 V logic levels with less than 1 ns transition times. Each output has a 50 Ω source impedance.

Timebases

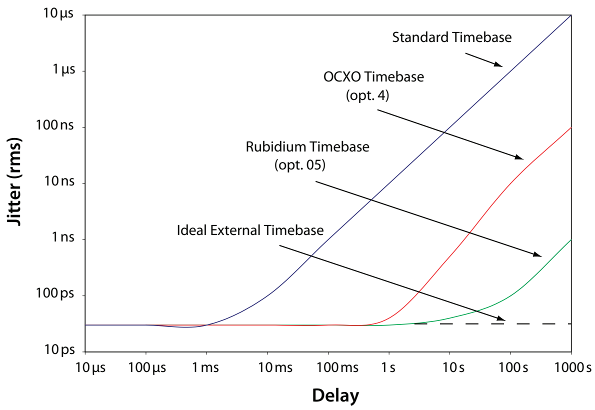
The standard time base has an accuracy of 5 ppm, and a jitter of 10^{-8}, which is suitable for many applications. Optional timebases are available for users who require better rate and delay accuracy or reduced rate and delay jitter.

The timing error for a 1 s delay can be as large as 5 µs for the standard timebase, 200 ns for the OCXO timebase, but is only 500 ps for the rubidium timebase (all 1 year after calibration.)



Timing error vs. programmed delay

For short delays the jitter is typically 20 ps. However, for a 1 s delay, the standard timebase can contribute up to 10 ns of jitter, while the optional timebases contribute less than 10 ps of additional jitter.



Jitter vs. programmed delay

DG645 (cover removed) with optional Rb timebase. Rear panel shows the optional eight-channel outputs.

Fast Rise Time Module

The DG645 front-panel outputs have transition times of less than 2 ns. The SRD1 is an accessory, built into an in-line BNC connector, which reduces the rise time of a front-panel output to less than 100 ps. Up to 5 SRD1s can be attached to the front panel to reduce the rise time of all of the outputs.

SRD1 Fast Rise Time Module

Ordering Information

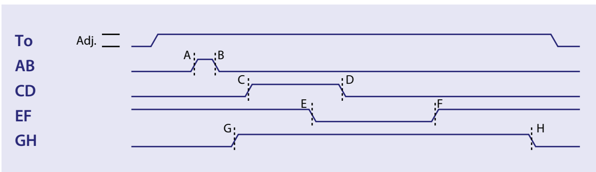
DG645	Delay/pulse generator	$3995
Option 01	Eight delay channels (5 V)	$750
Option 02	Eight delay channels (30 V)	$950
Option 03	Combinatorial outputs	$750
Option 04	OCXO timebase	$650
Option 05	Rubidium timebase	$1650
SRD1	100 ps rise time module	$250
O645RMS	Single rack mount kit	$85
O645RMD	Dual rack mount kit	$85

SRS Tech Note

More About the Outputs

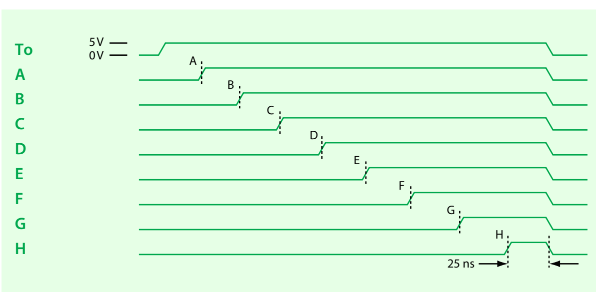
A timing cycle is initiated by an internal or external trigger. The T_0 output, whose leading edge is the zero-time reference, is asserted 85 ns after the trigger. The delay settings (A, B, C, D, E, F, G and H) determine the timing of the front-panel and rear-panel outputs.

The front-panel outputs have adjustable amplitude, offset, and polarity (non-inverted or inverted).



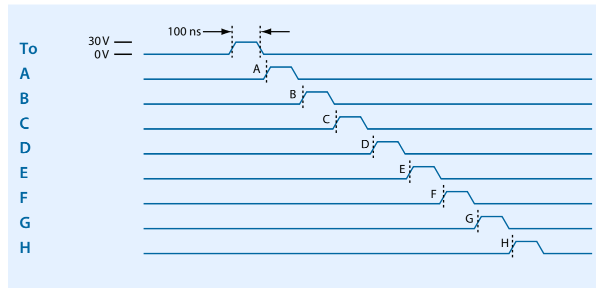
Front-panel outputs (adjustable)

Option 1 rear-panel outputs provide T_0 and eight delay outputs (A, B, C, D, E, F, G and H) to allow the DG645 to be used as an 8-channel delay generator. The outputs go from 0 to 5 V at their programmed delays, and return low 25 ns after the longest delay.



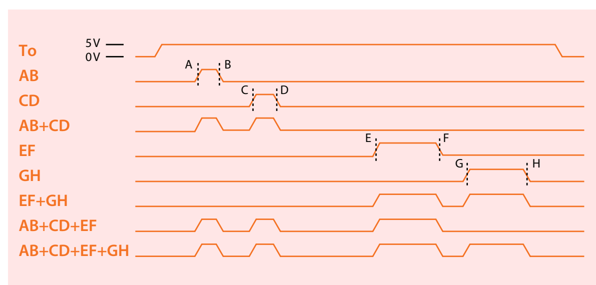
Opt. 1 rear-panel outputs (5 V)

Option 2 rear-panel outputs provide 30 V, 100 ns timing pulses at T_0, A, B, C, D, E, F, G and H. Output amplitudes are reduced to 15 V when driving 50 Ω loads.



Opt. 2 rear-panel outputs (30 V)

Option 3 rear-panel outputs provide outputs T_0, AB, CD, EF, GH (with the same definition as the front-panel outputs), and (AB+CD), (EF+GH), (AB+CD+EF), (AB+CD+EF+GH) which provide two, three, or four pulses per trigger.



Opt. 3 rear-panel combinatorial outputs (5 V)

DG645 rear panel with option 1 outputs

Delays

Channels	4 independent pulses controlled in position and width. 8 delay channels available as an option (see *Output Options*).
Range	0 to 2000 s
Resolution	5 ps
Accuracy	1 ns + (timebase error × delay)
Jitter (rms)	
Ext. trig. to any output	<25 ps + (timebase jitter × delay)
T_0 to any output	<15 ps + (timebase jitter × delay)
Trigger delay	85 ns (ext. trig. to T_0 output)

Timebases

Model #	Type	Jitter (s/s)	Stability (20 to 30 °C)	Aging (ppm/yr)
Std.	crystal	10^{-8}	2×10^{-6}	5
Opt. 4	OCXO	10^{-11}	1×10^{-9}	0.2
Opt. 5	Rb	10^{-11}	1×10^{-10}	0.0005

External input	10 MHz ± 10 ppm, sine >0.5 Vpp, 1 kΩ impedance
Output	10 MHz, 2 Vpp sine into 50 Ω

External Trigger

Rate	DC to 1/(100 ns + longest delay) (maximum of 10 MHz)
Threshold	±3.50 VDC
Slope	Trigger on rising or falling edge
Impedance	1 MΩ + 15 pF

Internal Rate Generator

Trigger modes	Continuous, line or single shot
Rate	100 μHz to 10 MHz
Resolution	1 μHz
Accuracy	Same as timebase
Jitter (rms)	<25 ps (10 MHz/N trigger rate) <100 ps (other trigger rates)

Burst Generator

Trigger to first T_0	
Range	0 to 2000 s
Resolution	5 ps
Period between pulses	
Range	100 ns to 42.9 s
Resolution	10 ns
Delay cycles per burst	1 to $2^{32} - 1$

Outputs (T_0, AB, CD, EF, and GH)

Source impedance	50 Ω
Transition time	<2 ns
Overshoot	<100 mV + 10 % of pulse amplitude
Offset	±2 V
Amplitude	0.5 to 5.0 V (level + offset <6.0 V)
Accuracy	100 mV + 5 % of pulse amplitude

General

Computer interfaces	GPIB (IEEE-488.2), RS-232, and Ethernet. All instrument functions can be controlled through the interfaces.
Non-volatile memory	Nine sets of instrument configurations can be stored and recalled.
Power	<100 W, 90 to 264 VAC, 47 Hz to 63 Hz
Dimensions	8.5 × 3.5 × 13 (WHD)
Weight	9 lbs.
Warranty	One year parts and labor on defects in materials & workmanship

Output Options

Option 1 (8 Delay Outputs on Rear Panel)

Outputs (BNC)	T_0, A, B, C, D, E, F, G and H
Source impedance	50 Ω
Transition time	<1 ns
Overshoot	<100 mV
Level	+5 V CMOS logic
Pulse characteristics	
Rising edge	At programmed delay
Falling edge	25 ns after longest delay

Option 2 (8 High-Voltage Delay Outputs on Rear Panel)

Outputs (BNC)	T_0, A, B, C, D, E, F, G and H
Source impedance	50 Ω
Transition time	<5 ns
Levels	0 to 30 V into high impedance 0 to 15 V into 50 Ω (amplitude decreases by 1 %/kHz)
Pulse Characteristics	
Rising Edge	At programmed delay
Falling Edge	100 ns after the rising edge

Option 3 (Combinatorial Outputs on Rear Panel)

Outputs (BNC)	T_0, AB, CD, EF, GH, (AB + CD), (EF + GH), (AB + CD + EF), (AB + CD + EF + GH)
Source impedance	50 Ω
Transition time	<1 ns
Overshoot	<100 mV + 10 % of pulse amplitude
Pulse characteristics	
T_0, AB, CD, EF, GH	Logic high for time between delays
(AB+CD), (EF+GH)	Two pulses created by the logic OR of the given channels
(AB+CD+EF)	Three pulses created by the logic OR of the given channels
(AB+CD+EF+GH)	Four pulses created by the logic OR of the given channels

Option SRD1 (Fast Rise Time Module)

Rise time	<100 ps
Fall time	<3 ns
Offset	0.8 V to 1.1 V
Amplitude	0.5 V to 5.0 V
Load	50 Ω