BERTScope™ S PG

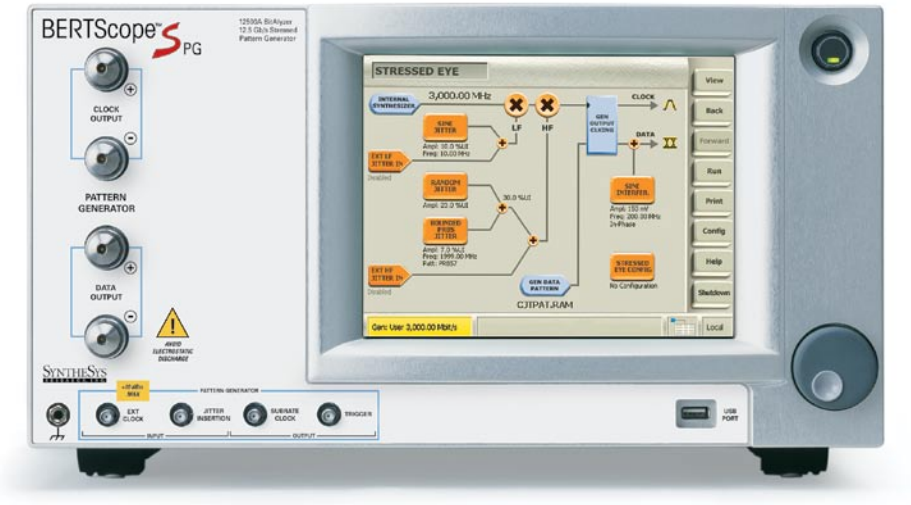
Stressed Pattern Generator

- Data generator from 0.1 to 12.5 Gb/s covering all popular high-speed standards
- Calibrated insertion of the following stress types:
  - Sinusoidal Jitter (SJ)
  - Sinusoidal Interference (SI)
  - Bounded Uncorrelated (PRBS) Jitter (BUJ)
  - Random Jitter (RJ)
- Differential outputs with exchangeable Planar Crown® connectors allowing change from APC-3.5 to other popular connector types
- Flexible sub-rate clock outputs with large selection of divider choices for driving devices under test
- Fast rise time of 25 ps typical (20 - 80%) with low jitter (< 1 ps rms typical)
- Stressing of an external clock, including one with Spread Spectrum Clocking (SSC) for serial bus testing
- Full-rate jittered clock output for driving additional legacy pattern generators for extra test flexibility
- Flexible pattern generation with intuitive RAM pattern editing and a library of common standards patterns such as Fibre Channel, Serial-ATA, etc

SYNTHESYS RESEARCH, INC.

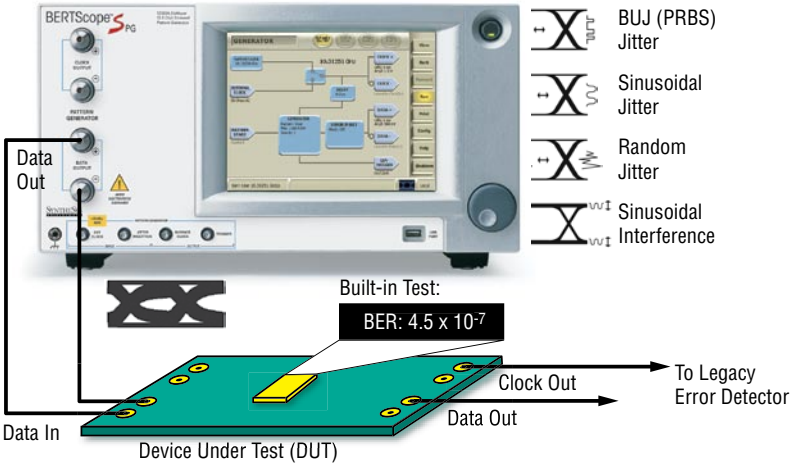
The Vision of a Scope, the Confidence of a BERT, and Clock Recovery you can Count on.

BERTScope™ SPG

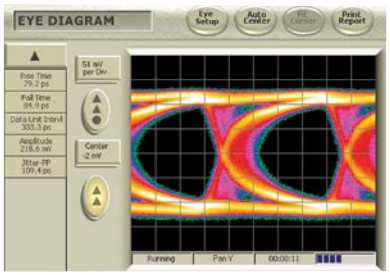


SyntheSys Research introduces the latest member of the BERTScope family. The BERTScope SPG is a BERTScope pattern generator with the ability to add stress impairments to an internal or external clock. This makes it a cost-effective solution for testing in applications where non-BER measurements are used to calibrate the DUT, and BER is measured by the DUT itself or a legacy BERT. This is also ideal for production testing where stress is to be set up for multiple test stations.

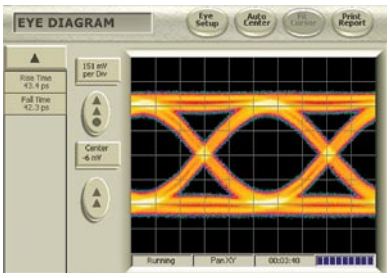
- Cost-effective stress generation for receiver jitter tolerance compliance testing for standards such as:
  - Serial ATA
  - FB-DIMM
  - PCI-Express
  - SAS
  - Fibre Channel 2x, 4x, 10x
  - 10 GbE
  - XFP/XFI
- The instrument provides calibrated amounts of common stress impairments. For ISI insertion there is the BERTScope Differential ISI Board to provide a known, well-behaved frequency response impairment unhindered by suck outs and other response issues associated with low-quality switching.
- External sinusoidal interference (SI) output may be used to drive a JDSU OPTX10 reference optical transmitter for 10 GbE receiver stress testing.



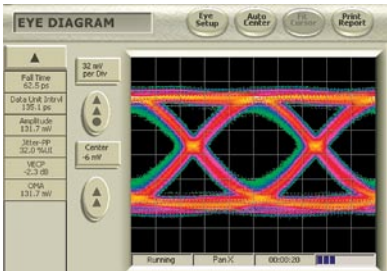
The BERTScope SPG is designed to make creating stress easy. It can be used cost-effectively in receiver testing where stress is required, and either the device being tested is able to measure errors, or the user wants to use an existing error detector instrument to count errors.



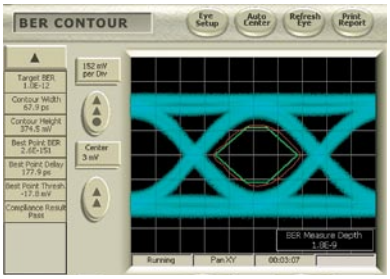
Compliant Serial-ATA stressed eye



Compliant 4x FC stressed eye



Compliant C' Input XFI stressed eye



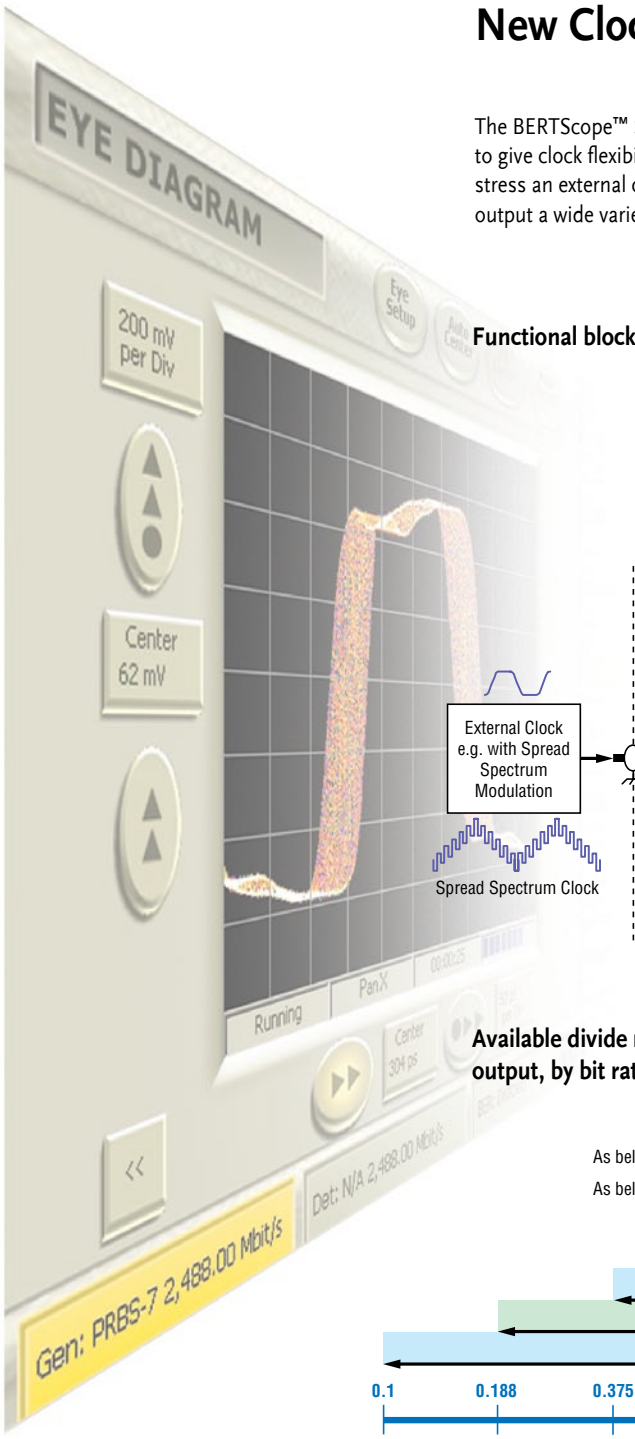
Same XFI stressed eye as above viewed as a BER Contour, showing that the 1x10^{-12} iso-BER line (red) passes the XFI mask (green).

Compliant stressed eyes for receiver jitter tolerance testing to the standards listed. These were measured at the point of application to the DUT using a BERTScope analyzer†.

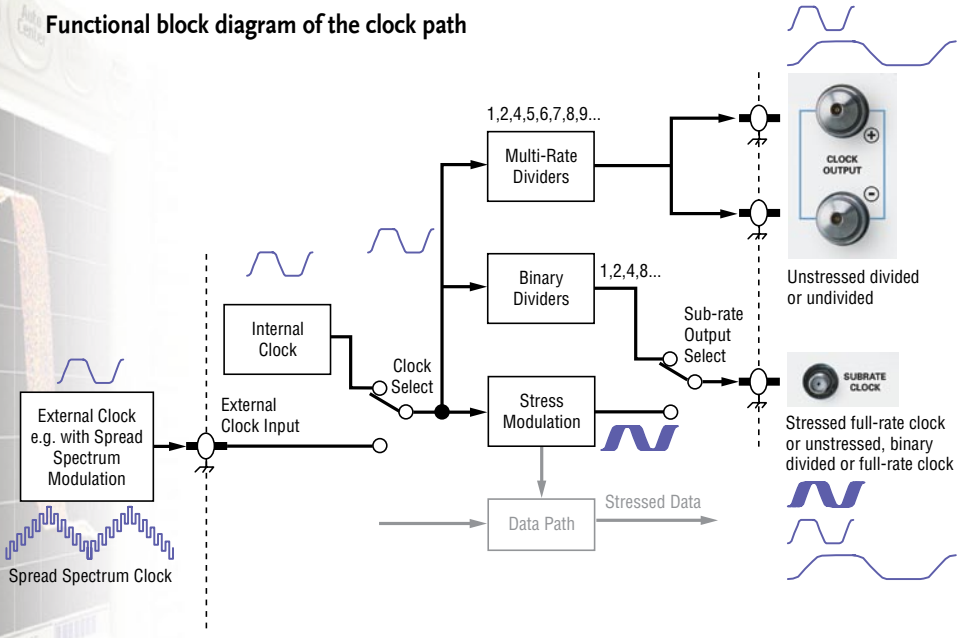
† In all cases, SyntheSys Research recommends calibration of the stressed eye using BER-related measurements at the device being tested to give the clearest picture of the signal the device will receive.

New Clocking Capabilities

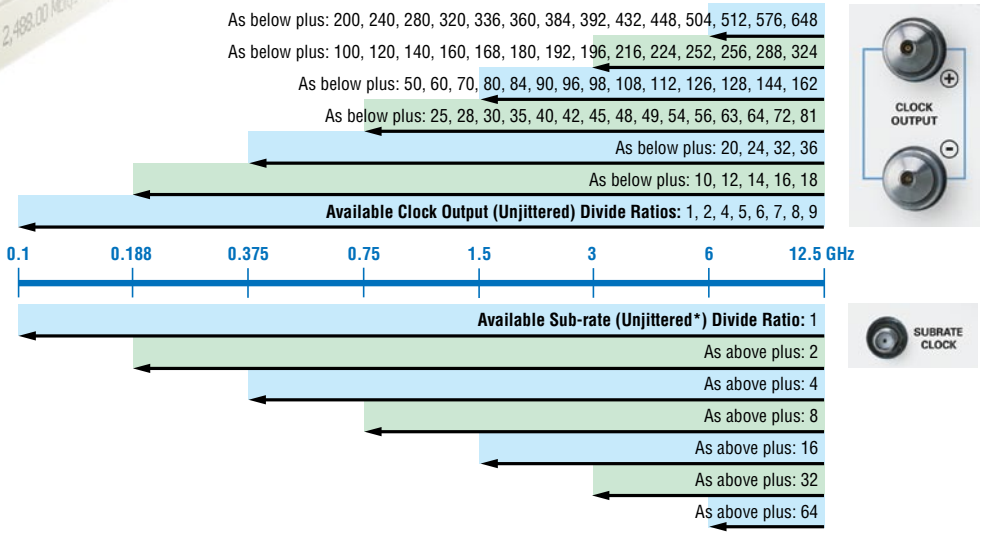
The BERTScope™ SPG has a number of new capabilities to give clock flexibility. These include the ability to stress an external clock, take incoming SSC, and output a wide variety of sub-rate clocks.



Functional block diagram of the clock path



Available divide ratios from clock-related output, by bit rate, using the internal clock†



* This output can also provide a full-rate Jittered clock.
† All listed ratios available for an external clock input over entire bit-rate range, limitations for internal clock only.

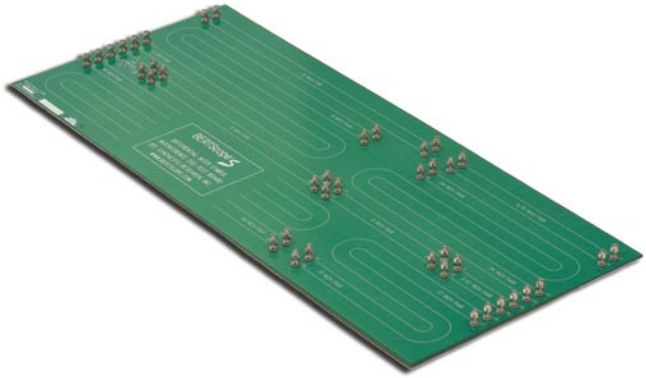
For more information on this and other products:

- BERTScope and BERTScope S Signal Integrity Analyzers Technical Specifications, SR-DS014
- BERTScope Family Brochure, SR-DS013
- BERTScope Differential ISI Board Product Brief, SR-DS018
- BERTScope CR Clock Recovery Instrument Product Brief, SR-DS016

Application information:

- Stressed Eye – Know what you are testing with, January 2006
- Constructing a 10 GbE Optical Fibre Channel Stressed Eye, January 2006
- Constructing a 4x FC Optical Stressed Eye, January 2006
- Testing the High Speed Electrical Specifications of an XFP Transceiver, July 2006
- Evaluating Stress Components Using BER-Based Jitter Measurements, September 2005

All available at www.bertscope.com



The BERTScope Differential ISI Accessory is an ideal companion to the BERTScope SPG, providing high quality, known frequency response impairment

About BERTScope™

BERTScope™ is a trademark of SyntheSys Reasearch, Inc. a privately held California corporation. Founded in 1989, its mission is to develop advanced test instruments for identifying and locating the source of errors in high-speed digital bit streams. BERTScope CR pairs with BERTScope to offer the vision of a scope, the confidence of a BERT, and clock recovery you can count on. More information is available at www.bertscope.com.

BERTScope™ S

The Vision of a Scope, the Confidence of a BERT, and Clock Recovery you can Count on.

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