

MP1800A Series

Signal Quality Analyzer



Anritsu MP1800A Signal Quality Analyzer

MP1800A
File View Help
12.50MHz FPO RF Module

Output Pattern Error Addition Misc

Data/Data OFF Clock/Clock OFF Offset Vch

Tracking OFF

Level Guard OFF

Setup

Offset	AC Off	DC Off	Scale
0.000 V	0.000 V	0.000 V	1.000 Vsp

External ATT Factor 0.000 dB

Amplitude 0.000 Vsp

Offset 0.000 V

Cross Point 50 %

Differential Skew 0 ps

Result Measurement Pattern Input Capture Misc

Going

Unit Time 00:00:00.01 Cycle Repeat

Current ON

Calculation Progressive Interval 100 ms

Error/Alarm

Zoom In Reset

2006.03.19 08:57:49

ER	TOTAL	INS	OMI
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EC

%EPI

EI

Frequency(kHz) 0 Clock Cause

Clock Loss

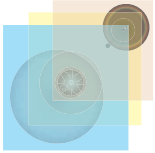
Sync Loss

Time

Data Threshold

XData Threshold

Going 0 %



Compact High-Performance 12.5 Gbit/s Signal Quality Analyzer

The increasingly widespread use of the Internet combined with the need for higher transmission capacities is leading to rapid development and deployment of devices for FTTx and 10G Ethernet. In addition, demand for faster data equipment interconnects is resulting in extensive R&D into high-speed circuits and transmission devices.

Device development and manufacturing inspection requires measuring instruments that can both send signals at various bit rates, levels, and patterns, as well as measure bit error rates in received signals.

The modular design of the MP1800A Signal Quality Analyzer (SQA) series offers customers a flexible cost-effective solution for performing measurements at the ideal bit error rate.

Expandable Slot Configuration

PON Module Upstream BER Test

Wideband 0.1 to 12.5 Gbit/s

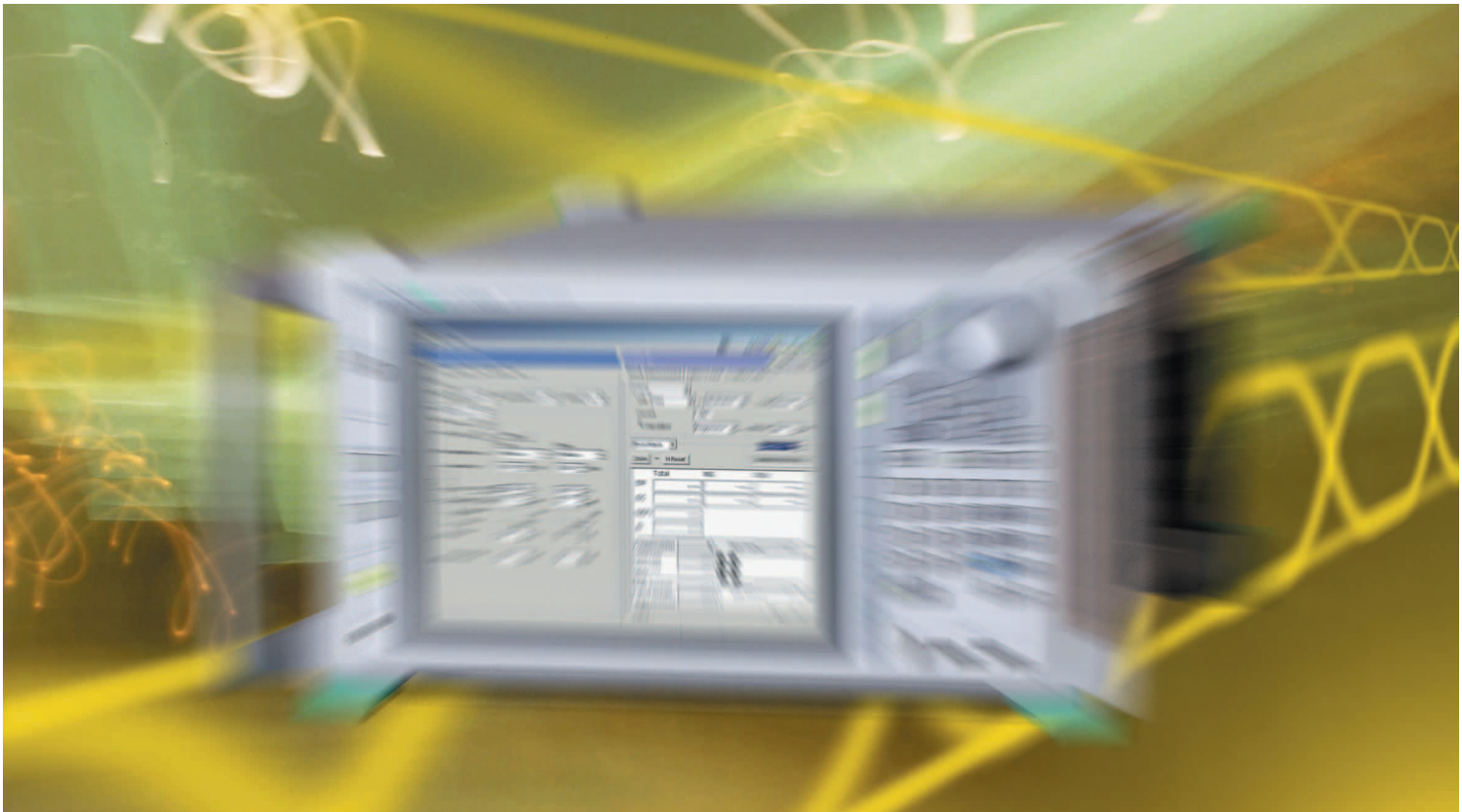
Wideband Clock Recovery

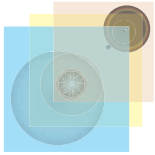
Differential Electrical Interface

Optical Interface

Mixed Pattern and Sequence Pattern

Multi Channel





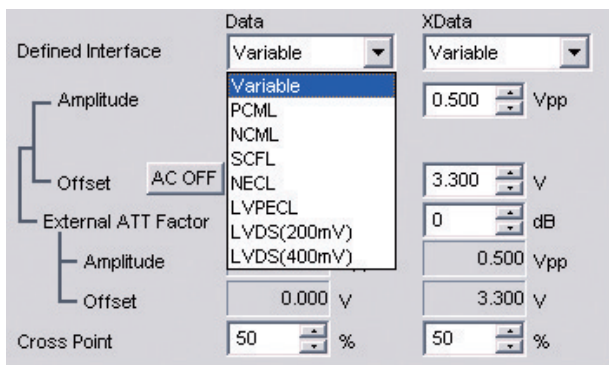
Main Features

Frequency Bands

- Both wideband and narrowband support
- 0.1 to 12.5 Gbit/s wide frequency band (MU181020A-002, MU181040A-002)
- 10 Gbit/s band of 9.8 to 12.5 Gbit/s (MU181020A-001, MU181040A-001)
- MU181020A-001 built-in clock generator
- PPG divided-clock function (1/2: 4.9 to 6.25 Gbit/s, 1/4: 2.45 to 3.125 Gbit/s, 1/8: 1.225 to 1.5625 Gbit/s)
- MU181040A-001 built-in clock recovery

Various Electrical Interfaces

- Variable/Fixed (PCML/NCML/SCFL/NECL/LVPECL/LVDS (200 mV)/LVDS (400 mV))



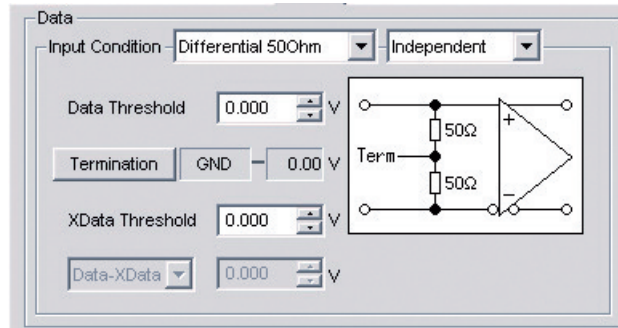
- Five Data Output Options
- Fixed 0/−0.5 V (MU181020A-001)
- Fixed 0/−1.0 V (MU181020A-002)
- Variable 0.05 to 0.8 Vp-p (MU181020A-010/110)
- Variable 0.25 to 2.5 Vp-p (MU181020A-011/111)
- High-performance 0.05 to 2.0 Vp-p (MU181020A-012/112)

High Input Sensitivity, Wide Phase Margin Data Input

- Input sensitivity <50 mVp-p (MU181040A-001)
- 10 mV typ. (MU181040A-002)
- Phase margin 60 ps typ. (@10 Gbits, PRBS2³¹−1, Single-end, Amplitude: 0.5 Vp-p) (MU181040A-002)

Differential Interface

- Supports both differential and single-end interfaces



Variable Phase Function

- PPG Variable Data Delay (± 1 UI) (MU181020A-030/130)
- Data Phase can be adjusted between each channel.
- ED Variable Clock Delay (± 1 UI) (MU181040A-030/130)

Optical Interfaces

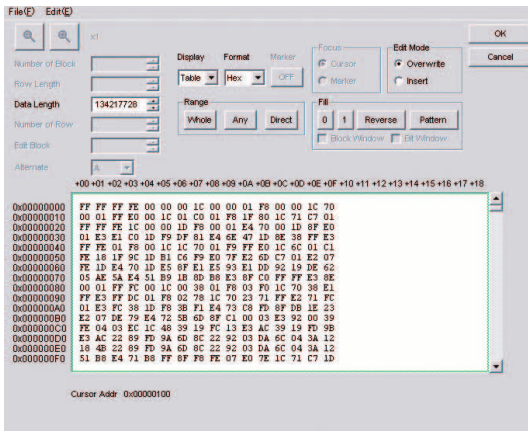
- Two optical interfaces: SFP and XFP
- Any wavelength from 850/1310/1550 nm supported by changing SFP/XFP optical transceiver

Full Line of Auxiliary Interfaces

- PPG AUX Input: Alternate Control/Sequence Trigger/Error Injection/Burst Trigger (Switchable)
- AUX Output: Divided clock/Pattern Sync
- Gating Output: Burst Trigger Output/Timing Signal
- ED AUX Input: Ext. Mask/Burst/Capture Ext. Trigger
- AUX Output: Divided clock/Pattern Sync/Sync Gain/Error Output

Full Pattern Line-up

- PRBS: 2^n-1 ($n=7, 9, 10, 11, 15, 20, 23, 31$)
- Zero-Substitute: $2^n, 2^n-1$ ($n=7, 9, 10, 11, 15, 20, 23$)
Pattern with continuous 0s or 1s appended to PRBS signals+1 bit
- DATA: Maximum 128 Mbits/1 bit step
- Alternate: Two types of pattern (A and B) using internal/External control timing alternately
- Mixed: Mixture of DATA and PRBS pattern
- Sequence: Several provided programmable patterns in set sequence



Various BER Measurement Functions

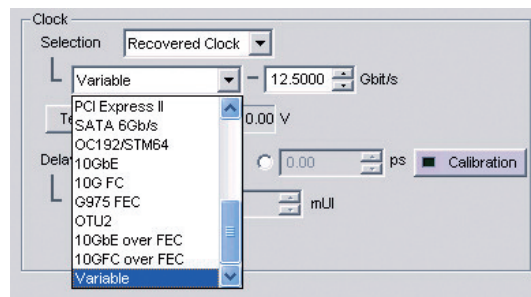
- General-purpose BER measurement (Total/Insertion/Omission)
- Signal Transition/Non-Transition BER measurement
- Eye margin/Eye diagram/Q measurement/Bathtub/ISI
- Input signal capture (128 Mbits)

Burst BER Measurement

- PON (OLT/ONU) Module tests
Supplies signals (Data/Pre-Bias/Reset) required for upstream tests
- Optical Recirculation Loop Test

Wideband Variable Clock Recovery Function

- MU181040A-001
9.8 to 12.5 GHz
 - MU181040A-002 with MU181040A-020/120
0.1 GHz, 0.125 to 0.2 GHz, 0.25 to 0.4 GHz, 0.5 to 0.8 GHz, 1 to 1.6 GHz, 2 to 3.2 GHz, 4.25 GHz, 4.9 to 6.25 GHz, 9.8 to 12.5 GHz
- OC3/STM1, OC12/STM4, 1GFC, GbE, SATA 1.5 Gb/s, 2GFC, OC48/STM16, PCI Express I, OTU1, SATA 3 Gb/s, XAUI, 4GFC, PCI Express II, SATA 6 Gb/s, OC192/STM64, 10 GbE, 10GFC, G975 FEC, OTU2, 10 GbE w/FEC, 10GFC w/FEC



Multi-channel Support

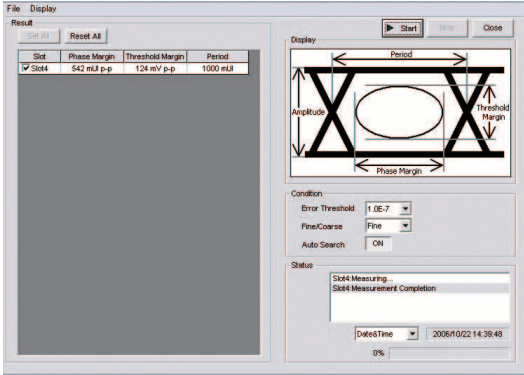
- Supports parallel interfaces
- Pattern synchronous and asynchronous operation between parallel channels
- 6-slot (MP1800A) and 4-slot (MT1810A) chassis types
 - MP1800A: Analyzer with integrated TX/RX for R&D and manufacturing; uses Windows® XP GUI for intuitive GUI operation
 - MT1810A: Compact main frame for manufacturing
Easy to configure for production lines
- Up to four PPG or ED modules can be installed and a 43.5 Gbit/s BERTS can be configured when used in combination with the Anritsu 43.5 Gbit/s MUX/DEMUX
- User changeable modules

Remote Control

- Control via GPIB/Ethernet
- High compatibility with remote commands used by previous model

Eye Margin

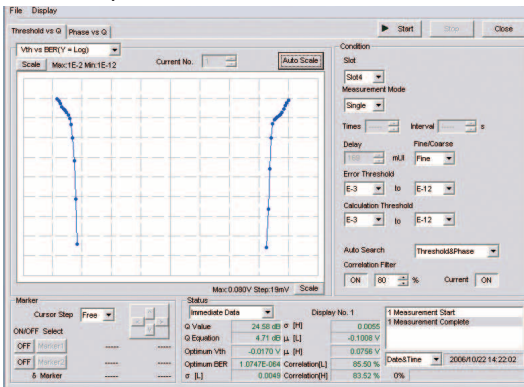
For confirming DATA threshold and phase margins.



* Please refer the "Selection Guide for Error Detector's Functions" on the 14 pages.

Q Measurement

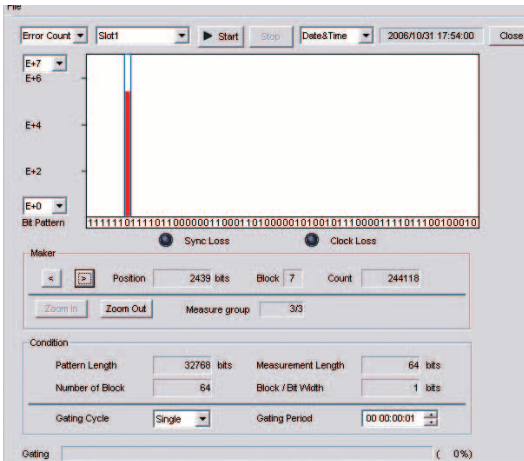
Calculates Q value from bit error rate using change in threshold value. Can be used to check change in Q value for clock phase.



* Please refer the "Selection Guide for Error Detector's Functions" on the 14 pages.

Bit Error Analysis using ISI

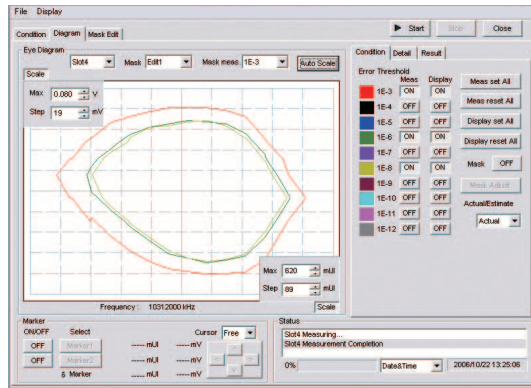
Used to confirm bit error rate in each specified block or bit position and for bit error rate correlation with inter-symbol interference.



* Please refer the "Selection Guide for Error Detector's Functions" on the 14 pages.

Eye Diagram

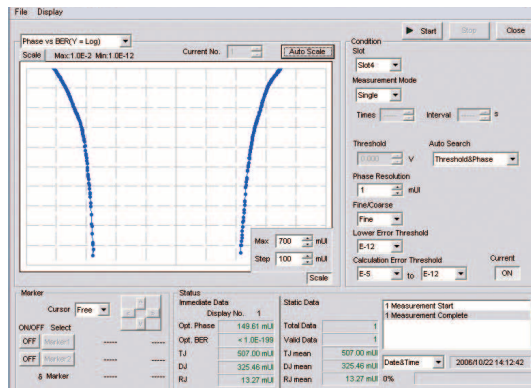
Used to obtain bit error rate contours linking specified bit error rate points.



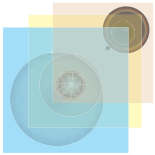
* Please refer the "Selection Guide for Error Detector's Functions" on the 14 pages.

Bathtub

Performs jitter analysis based on changes in bit error rate relative to phase.

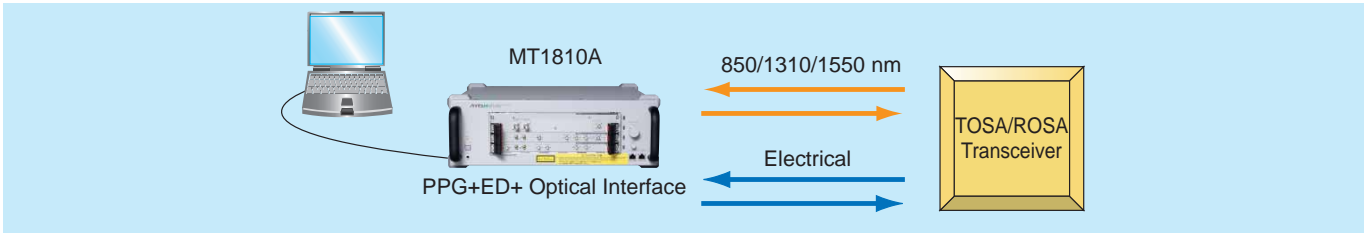


* Please refer the "Selection Guide for Error Detector's Functions" on the 14 pages.



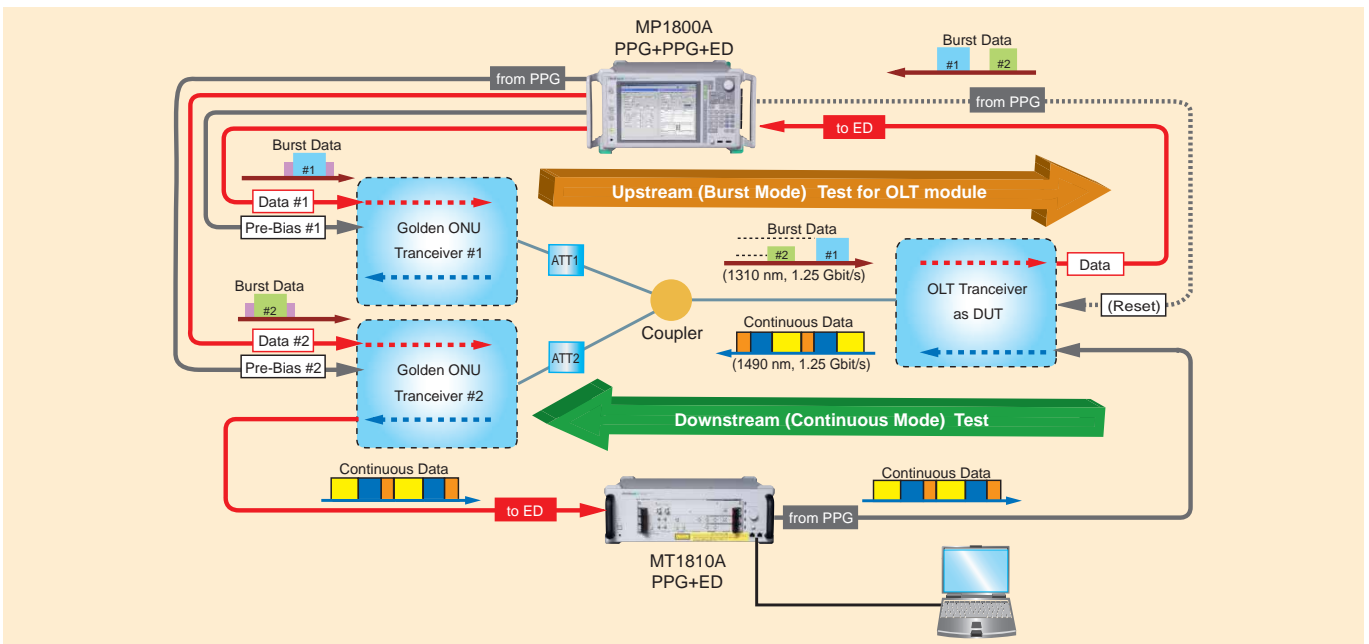
Applications

Application 1 Manufacturing Inspection of 10 Gbit/s Devices



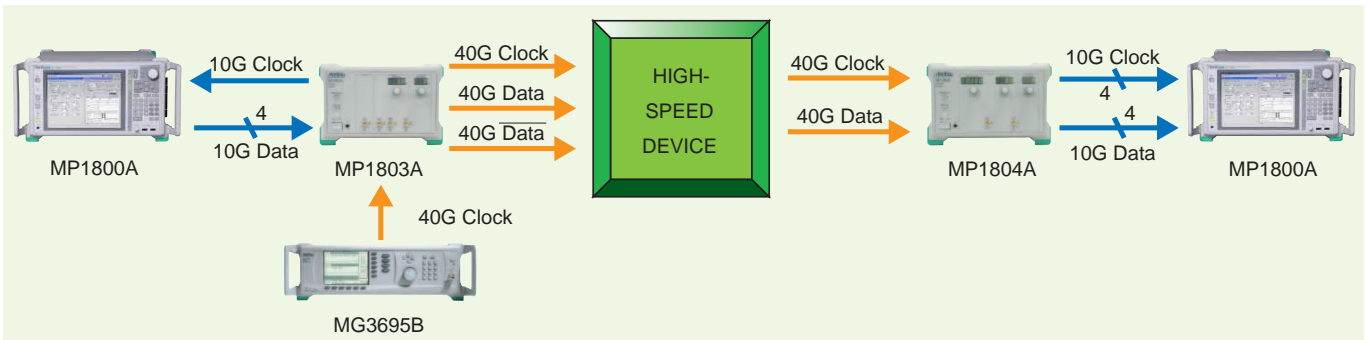
- A measurement system can be configured with no external clock source using the PPG 9.8 to 12.5 Gbit/s option. (MU181020A-001)
- Various wavelengths and bit rates can be defined by changing XFP modules in the optical transceiver slot.

Application 2 10 Gbit/s PON OLT Module Inspection

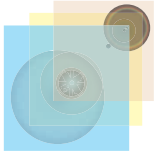


- Each PPG slot can output pre-bias and reset signals for the PON BER test. (Level: H: 0 V; L: -1 V)
- The PON OLT Upstream test can be performed at up to 12.5 Gbit/s using one MP1800A.

Application 3 Evaluation of 43.5 Gbit/s High-speed Devices



- A 4-channel PPG and 4-channel ED are used in combination with the Anritsu 43.5 Gbit/s MUX/DEMUX to function as a 43.5 Gbit/s BERTS.
- A PPG with the MU181020A-030/130 (installed in MU181020A-002) Variable Data Delay is installed to synchronize with other PPGs.



External Appearance

MP1800A 6-slot Main Frame

- Screen-based operation using Windows® XP GUI or remote commands over GPIB or Ethernet.
- The 6-slot main frame accommodates a combination of synthesizer, PPG, ED, and Optical Interface modules (The synthesizer module uses 2 slots).
- 4-channel PPG or ED operation is also supported when the MU181020A-030/130 is installed.

When used in combination with the Anritsu 43.5 Gbit/s MUX/DEMUX, the analyzer can function as a 43.5 Gbit/s BERTS.

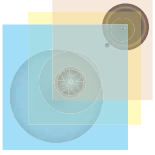
- Optimum cost performance is achieved by selecting the right main frame with the number of slots required for the PPG and /or ED modules (MP1800A-014/015/016).



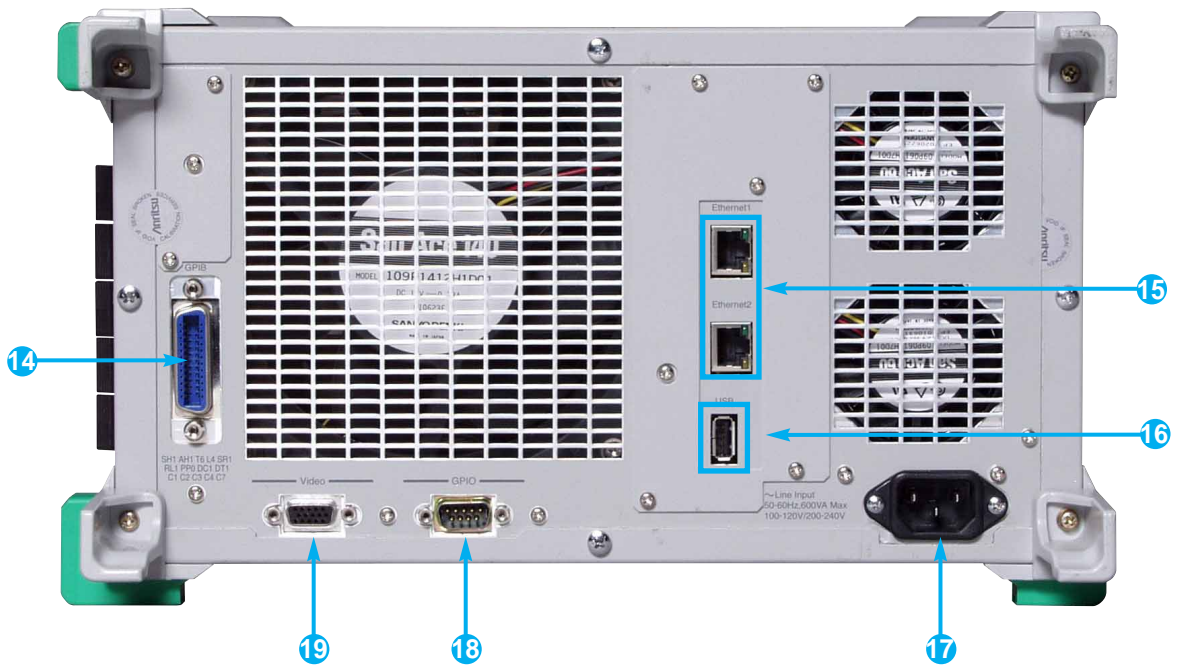
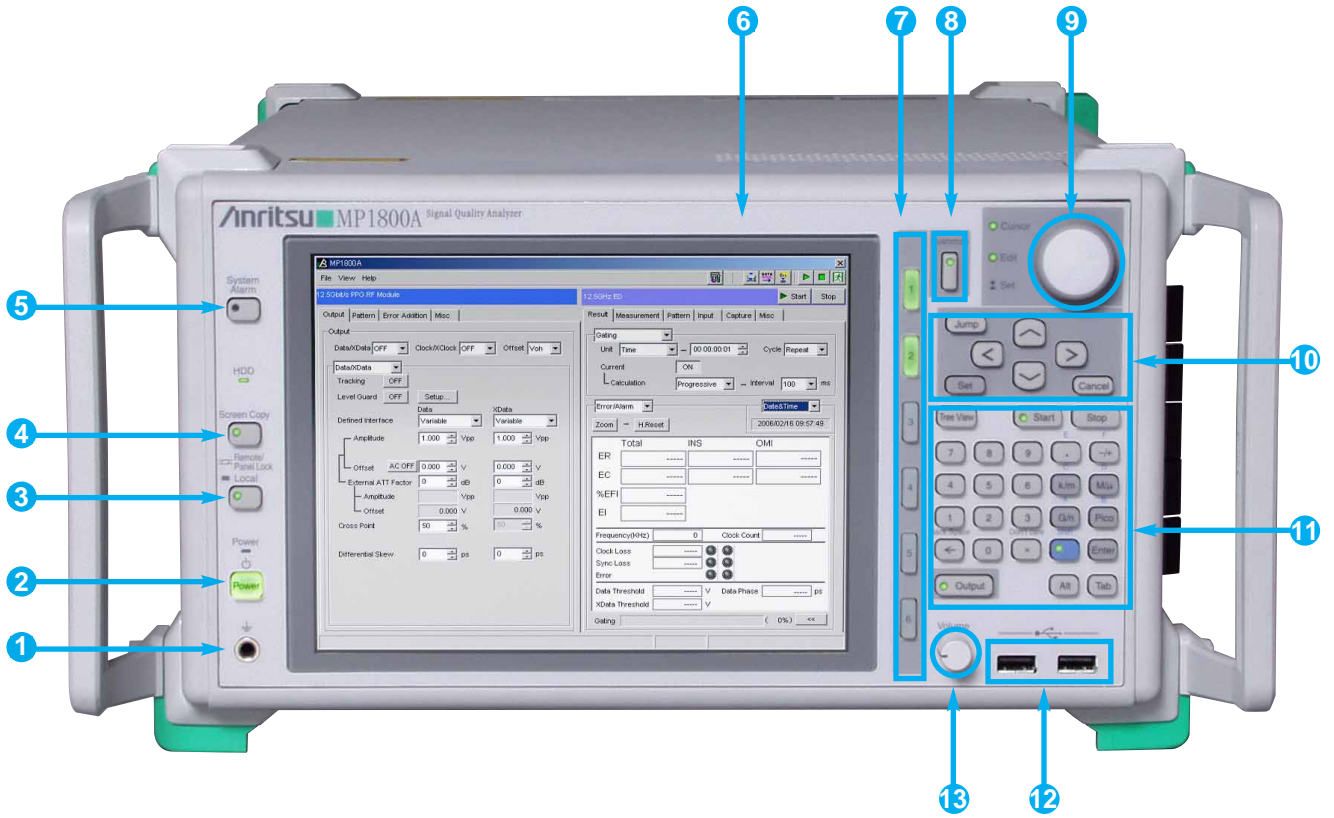
MT1810A 4-slot Main Frame

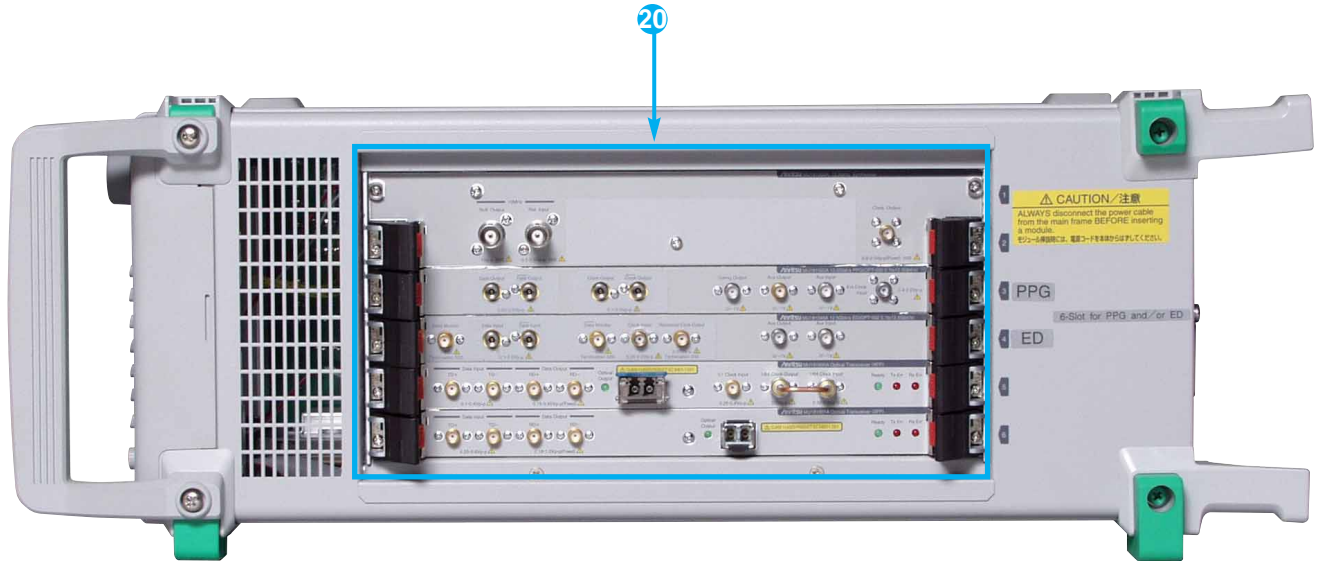
- Dedicated applications can be run from an external PC.
- Up to four units can be daisy chained and controlled by one PC.
- MX180000A can be remote controlled from the same PC with customer installed software.
- Ideal for inspecting 10 Gbit/s devices at 0.1 to 12.5 Gbit/s
- Optimum cost performance is achieved by selecting the right main frame with the number of slots required for the PPG and/or ED modules (MT1810A-014/015).



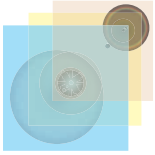


MP1800A Signal Quality Analyzer

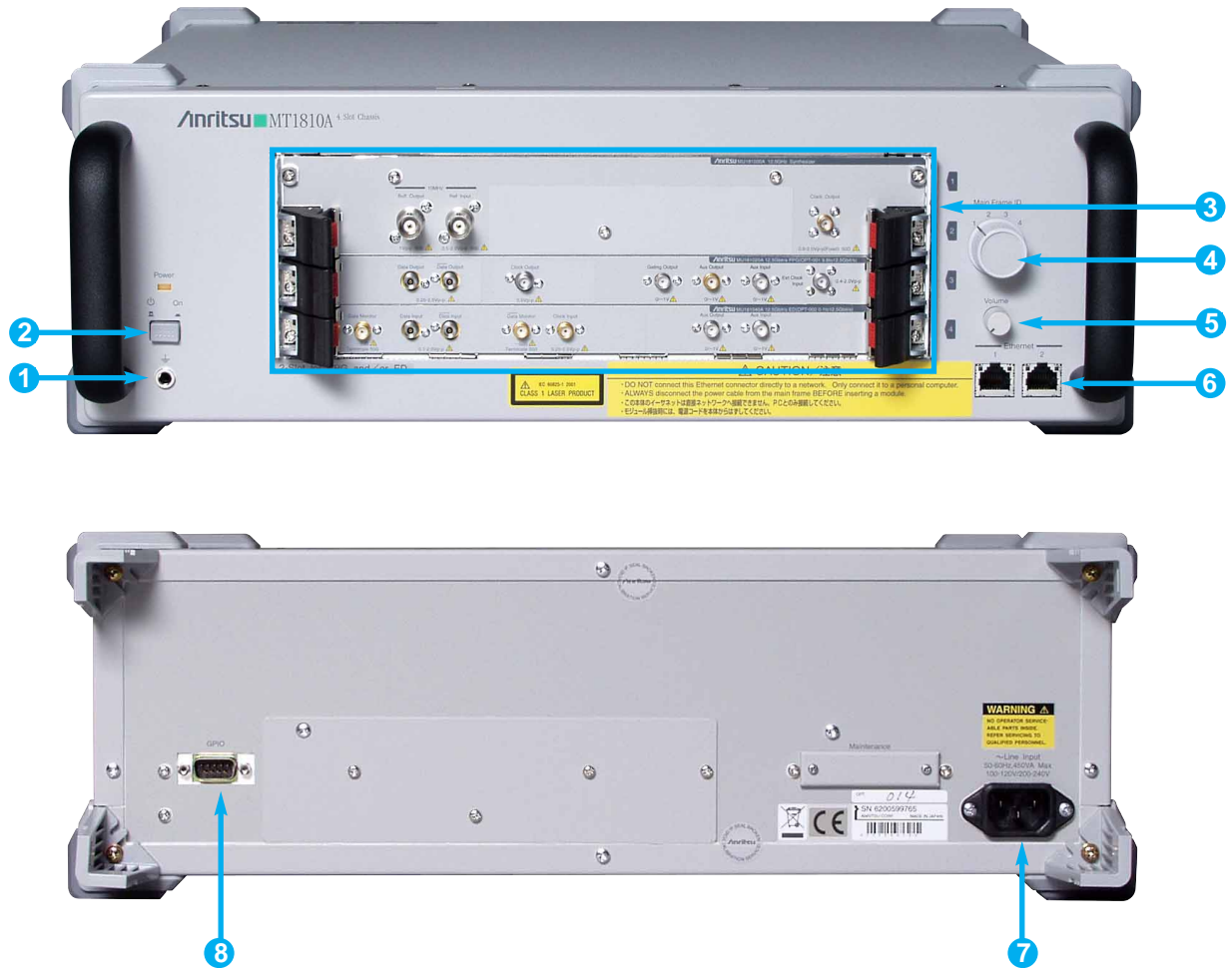




- 1 Ground**
This terminal is used to discharge static electricity.
- 2 Power**
This switches the unit power on and off.
- 3 Panel Lock/Remote**
This key locks the panel operation keys.
- 4 Screen Copy**
This key prints the currently displayed screen at a connected external printer.
- 5 System Alarm**
The key LED lights at a system error and a dialog explaining the error contents is displayed.
- 6 Display**
8.4-inch Color TFT 800 x 600
- 7 Slot Keys**
These keys correspond to the operation screen for each installed module.
- 8 Customize Key**
This key is used to call up to eighteen commonly used screens.
- 9 Rotary encoder**
When the [Edit] key lamp is lit, turning this rotary encoder increases or decreases numeric values. When the [Cursor] key lamp is lit, the operation item can be set. Press the rotary encoder to switch between the [Edit] and [Cursor] functions.
- 10 Cursor Key**
These keys move the screen cursor up, down, left and right on screen.
- 11 Ten Key**
These ten keys are for inputting numeric values, units, etc.
- 12 USB**
Two Rev. 1.1 USB ports
- 13 Volume**
This knob increases and decreases the volume of the measurement error alarm.
- 14 GPIB**
This connector is used when the MP1800A-001 GPIB option is installed.
- 15 Ethernet**
This unit has two RJ45 Ethernet jacks supporting connection to 10 BASE-T or 100 BASE-TX cables.
- 16 USB**
Rev. 1.1 USB port
- 17 Inlet**
This socket is for connecting the 3-wire power cord.
- 18 GPIO**
Reserved for future use
- 19 VIDEO**
This connector is for an external display.
- 20 Slots for modules**
These slots are for installing up to six modules.

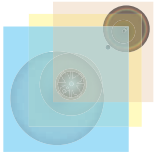


MT1810A 4Slot Chassis



- 1 Ground**
This terminal is used to discharge static electricity.
- 2 Power**
This switches the unit power on and off.
- 3 Slots for modules**
These slots are for installing up to four modules.
- 4 Mainframe ID**
Used to identify the MT1810A units when multiple (up to 4) MT1810A units are connected.

- 5 Volume**
This knob increases and decreases the volume of measurement error alarm.
- 6 Ethernet**
This unit has two RJ45 Ethernet jacks supporting connection to 10 BASE-T or 100 BASE-TX cables.
- 7 Inlet**
This socket is for connecting the 3-wire power cord.
- 8 GPIO**
Reserved for future use



MP1800 Series Modules

• MU181000A 12.5 GHz Synthesizer



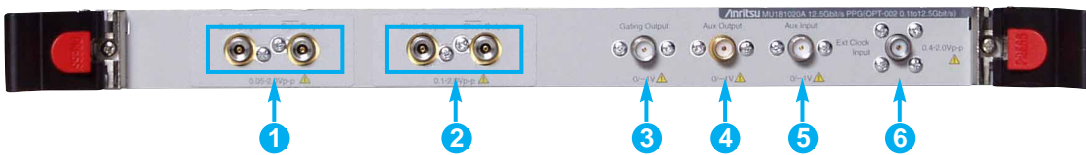
- 1 10 MHz Buff Output: Output for 10 MHz reference clock
- 2 10 MHz Ref. Input: Input for 10 MHz reference clock
- 3 Clock Output: Clock output

• MU181800A 12.5 GHz Clock Distributor

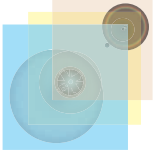


- 1 Clock Output 1 to 4: Output for divided clock of Clock Input
- 2 Clock Input: Clock input

• MU181020A 12.5 Gbit/s PPG

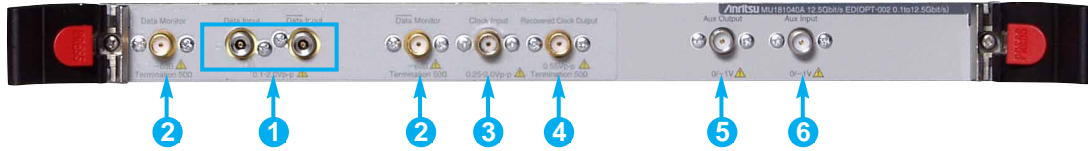


- 1 Data/Data Output: Output for differential data signal
- 2 Clock/Clock Output: Output for differential clock signal (single-end output without output option) (MU181020A-021, 121)
- 3 Gating Output: Output for burst timing signal
- 4 Aux Output: Output for auxiliary signal
- 5 Aux Input: Input for auxiliary signal
- 6 Ext. Clock Input: Clock input



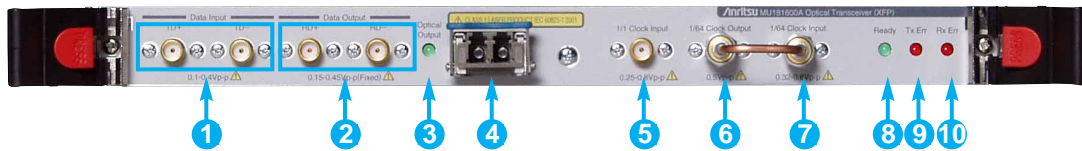
MP1800 Series Modules

● MU181040A 12.5 Gbit/s ED



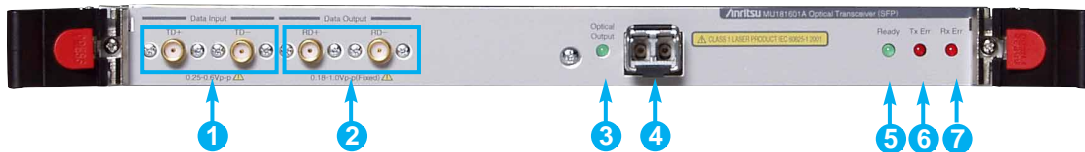
- 1 Data/Data Input: Input for differential data signal
- 2 Data/Data Monitor: Output for divided clock of input data (only enabled when 0.1 to 12.5 Gbit/s option (MU181040A-002) installed)
- 3 Clock Input: Clock input (only enabled when 0.1 to 12.5 Gbit/s option (MU181040A-002) installed)
- 4 Recovered Clock Output: Output for regenerated clock from input data (only enabled when MU181040A-020/120 installed)
- 5 Aux Output: Output for auxiliary signal
- 6 Aux Input: Input for auxiliary signal

● MU181600A Optical Transceiver (XFP)

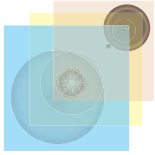


- 1 TD+/TD- Data Input: Input for electrical signal to XFP module
- 2 RD+/RD- Data Output: Output for electrical signal output from XFP module
- 3 Optical Output (LED): Displays XFP module optical signal status
- 4 Slot for Module: Slot for XFP module
- 5 1/1 Clock Input: Input for 1/1 clock
- 6 1/64 Clock Output: Output for 1/64 clock of 1/1 clock input
- 7 1/64 Clock Input: Input for 1/64 reference clock
- 8 Ready (LED): Displays XFP module installation status
- 9 Tx Err (LED): Displays XFP transmitter error status
- 10 Rx Err (LED): Displays XFP receiver error status

● MU181601A Optical Transceiver (SFP)



- 1 TD+/TD- Data Input: Input for electrical signal to SFP module
- 2 RD+/RD- Data Output: Output for electrical signal output from SFP module
- 3 Optical Output: Displays SFP module optical signal status
- 4 Slot for Module: Slot for SFP module
- 5 Ready (LED): Displays SFP module installation status
- 6 Tx Err (LED): Displays SFP transmitter error status
- 7 Rx Err (LED): Displays SFP receiver error status



Composition

Category	Model	Function	Note
Main Frame	MP1800A	Signal Quality Analyzer 6 slots with Windows® XP GUI	—
	MP1800A-001	GPIO	
	MP1800A-002	LAN	
	MP1800A-014*1	Max. of 2 PPG and/or ED	Must choose one from -014, -015 and -016
	MP1800A-015*1	Max. of 4 PPG and/or ED	
	MP1800A-016*1	Max. of 6 PPG and/or ED	
	MT1810A	4 Slot Chassis 4 slots controlled from external PC	—
	MT1810A-014*1	Max. of 2 PPG and/or ED	Must choose one from -014 and -015
MT1810A-015*1	Max. of 4 PPG and/or ED		
Clock Generator	MU181000A	12.5 GHz Synthesizer (0.1 to 12.5 GHz)	—
	MU181800A	12.5 GHz Clock Distributor (0.1 to 12.5 GHz)	
Pulse Pattern Generator (PPG)	MU181020A	12.5 Gbit/s PPG	—
	MU181020A-001	Narrowband (9.8 to 12.5G) differential 0 /-0.5 V fixed level External clock source not required Multi-channel syncing not required Operation bit rates: 9.8 to 12.5 Gbit/s 4.9 to 6.25 Gbit/s 2.45 to 3.125 Gbit/s 1.225 to 1.5625 Gbit/s	Must choose one from -001 and -002
	MU181020A-002	Wideband (0.1 to 12.5 G) differential 0/-1.0 V fixed level MU181000A or external clock source required	
	MU181020A-021*2 MU181020A-121*3	Differential Clock Output (0.1 to 2.0 Vp-p)	—
	MU181020A-030*2 MU181020A-130*3	Variable Data Delay (± 1 UI)	Install in -002 Required for parallel syncing
	MU181020A-010*2 MU181020A-110*3	Variable Data Output (0.05 to 0.8 Vp-p)	Choose one from -010/110, -011/111 and -012/112
	MU181020A-011*2 MU181020A-111*3	Variable Data Output (0.25 to 2.5 Vp-p)	
	MU181020A-012*2 MU181020A-112*3	High Performance Data Output (0.05 to 2.5 Vp-p)	
Error Detector (ED)	MU181040A	12.5 Gbit/s ED	—
	MU181040A-001	Narrowband differential data input (9.8 to 12.5 Gbit/s)	Must choose one from -001 and -002
	MU181040A-002	Wideband differential data input (0.1 to 12.5 Gbit/s)	
	MU181040A-020*2 MU181040A-120*3	Clock Recovery: 0.1 GHz, 0.125 to 0.2 GHz, 0.25 to 0.4 GHz, 0.5 to 0.8 GHz, 1 to 1.6 GHz, 2 to 3.2 GHz, 4.25 GHz, 4.9 to 6.25 GHz, 9.8 to 12.5GHz	Install in -002*6
	MU181040A-030*2 MU181040A-130*3	Variable Clock Delay (± 1 UI)	Install in -002
Optical Interface	MU181600A*4	Optical Transceiver (XFP)	—
	MU181601A*5	Optical Transceiver (SFP)	

*1: Option specifying max.number of inserted PPG and ED modules and slot positions.

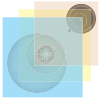
*2: Original order option

*3: Upgrade option to original order

*4: XFP module sold separately

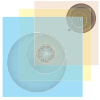
*5: SFP module sold separately

*6: We recommend adding the option of MU181040A-030/130 Variable Clock Delay to perform the tests with the best phase condition when using MU181040A-020/120 Clock Recovery.



Selection Guide for Error Detector's Functions

Function	Model Name	MU181040A		
	Frequency option	MU181040A-002		MU181040A-001
	Delay Option	MU181040A-030	—	—
Auto Search	Threshold	Supported	Supported	Not Supported
	Phase	Supported	Not Supported	Not Supported
Auto Adjustment	Threshold	Supported	Supported	Supported
	Phase	Supported	Not Supported	Not Supported
Eye Margin	Threshold	Supported	Supported	Not Supported
	Phase	Supported	Not Supported	Not Supported
Eye Diagram		Supported	Not Supported	Not Supported
Bathtub		Supported	Not Supported	Not Supported
Q Measurement		Supported	Not Supported	Not Supported
ISI Analysis		Supported	Supported	Supported

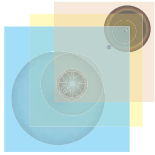


Comparison with Previous Model

Category	MP1800 Series	MP1763/64C
Operating Frequency	0.1 to 12.5 GHz	0.05 to 12.5 GHz
Test Pattern	PRBS, Zero_sub, PRGM, ALT, Mixed, Sequence	PRBS, Zero_sub, PRGM, ALT
Data Length	128 Mbit	8 Mbit
Mixed Pattern	Supported	Not Supported
Sequence Pattern	Supported	Not Supported
Data Output	0/-0.5 V (MU181020A-001) 0/-1.0 V (MU181020A-002) 0.05 to 0.8 Vp-p (MU181020A-010/110) 0.25 to 2.5 Vp-p (MU181020A-011/111) 0.05 to 2.0 Vp-p (MU181020A-012/112)	0.25 to 2.0 Vp-p
Delay	All of bit rate ± 1 UI, Steps:1 mUI	-500 to +500 ps, Steps: 1 ps
Sync Output	Pattern Sync 1/N Clock (MU181020A-002: N=2, 4, 8 to 511) (MU181040A-002: N=8 to 511)	Pattern Sync 1/64 Clock
Data Input sensitivity	10 mVp-p typ.	≤ 50 mVp-p
Clock Recovery (Option)*2	0.1 to 3.2 GHz, 4.25 GHz, 4.9 to 6.25 GHz, 9.8 to 12.5 GHz	62.5 MHz to 3.2 GHz, 4.25 GHz, 9.95 to 11.0 GHz
Logging, Histogram	Error Logging function	Not Supported
Eye Margin	Supported	Supported
Eye Diagram	Supported	Supported
Q Measurement	Supported	Supported
Bathtub	Supported	Not Supported
ISI	Supported	Not Supported
Auto Search	Supported	Supported
Auto Adjust	Supported	Not Supported
Capture	128 Mbit	256 bit
FPGA Upgradability	Supported	Not Supported
Remote Function	Ethernet, GPIB	GPIB
Multi-channel	4/6 slot	Not Supported
Optical Interface	Supported	Not Supported

*1: Using external PC with application software.

*2: We recommend adding the option of MU181040A-030/130 Variable Clock Delay to perform the tests with the best phase condition when using MU181040A-020/120 Clock Recovery.

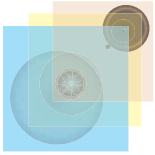


Selection Guide

Category	Model Name/Function	10G Device	10G PON OLT Downstream	10G PON OLT Upstream	4ch PPG (without clock)	4ch ED	High-performance PPG	General purpose PPG + ED (without CDR)
Main Frame	MP1800A Signal Quality Analyzer			√	√			√
	MP1800A-014 Max. of 2 PPG and/or ED							√
	MP1800A-015 Max. of 4 PPG and/or ED			√	√			
	MP1800A-016 Max. of 6 PPG and/or ED							
	MT1810A 4 Slot Chassis	√	√			√	√	
	MT1810A-014 Max. of 2 PPG and/or ED	√	√				√	
	MT1810A-015 Max. of 4 PPG and/or ED					√		
Clock Generator	MU181000A 12.5 GHz Synthesizer		√	√			√	√
	MU181800A 12.5 GHz Clock Distributor			√	√			
Pulse Pattern Generator (PPG)	MU181020A 12.5 Gbit/s PPG	√	√	√ *1	√ *2		√	√
	MU181020A-001 9.8 to 12.5 Gbit/s Built-in Clock	√						
	MU181020A-002 0.1 to 12.5 Gbit/s MU181000A or external clock source is required		√	√ *1	√ *2		√	√
	MU181020A-021/121 Differential Clock Output						√	
	MU181020A-030/130 Variable Data Phase Shift Parallel Syncing		√	√ *1	√ *2		√	√
	MU181020A-010/110 Data Output 0.05 to 0.8 Vp-p			√ *1				
	MU181020A-011/111 Data Output 0.25 to 2.5 Vp-p							√
	MU181020A-012/112 Data Output 0.05 to 2.0 Vp-p						√	
Error Detector(ED)	MU181040A 12.5G bit/s ED	√	√	√		√ *2		√
	MU181040A-001 9.8 to 12.5 Gbit/s Clock Recovery included	√						
	MU181040A-002 0.1 to 12.5 Gbit/s		√	√		√ *2		√
	MU181040A-020/120 Clock Recovery							
	MU181040A-030/130 Variable Clock Delay		√	√		√ *2		√
Optical Interface	MU181600A Optical Transceiver (XFP)	√						
	MU181601A Optical Transceiver (SFP)							

*1: Please add the number as needed.

*2: To configure 4ch PPG/ED, each of 4 modules and 4 options are needed.



Specifications

● MP1800A Signal Quality Analyzer

LCD Display	8.4-inch Color TFT 800 x 600
Peripheral I/Fs	VGA out (SVGA), USB 1.1 (3 Ports)
Remote Interface	MP1800A-001 GPIB, MP1800A-002 LAN (2 ports)
Options	MP1800A-014: Max. of 2 PPG and/or ED; MP1800A-015: Max. of 4 PPG and/or ED; MP1800A-016: Max. of 6 PPG and/or ED
Power	100 to 120 Vac, 200 to 240 Vac (auto-switching between 100/200 Vac), 47.5 to 63 Hz
Power Consumption	≤600 VA
Operating Temperature	+5° to +40°C
Dimensions and Mass	320 mm (W) x 177 mm (H) x 450 mm (D), ≤13 kg max. (without modules)
EMC	EN61326:1997+A1:1998+A2:2001+A3:2003 (Class A, Annex A), EN61000-3-2: 2000 (Class A)
LVD	EN61010-1:2001 (Pollution Degree 2)

● MT1810A 4 Slot Chassis

Remote Interface	LAN (2 ports)
Options	MT1810A-014: Max. of 2 PPG and/or ED; MT1810A-015: Max. of 4 PPG and/or ED
Power	100 to 120 Vac, 200 to 240 Vac (auto-switching between 100/200 Vac), 47.5 to 63 Hz
Power Consumption	≤450 VA
Operating Temperature	+5° to +40°C
Dimensions and Mass	350 mm (W) x 132.5 mm (H) x 400 mm (D), 13 kg max. (without modules)
EMC	EN61326:1997+A1:1998+A2:2001+A3:2003 (Class A, Annex A), EN61000-3-2: 2000 (Class A)
LVD	EN61010-1:2001 (Pollution Degree 2)

● MU181000A 12.5 GHz Synthesizer

Frequency Range	0.1 to 12.5 GHz, 1 kHz/1 MHz steps Offset from set frequency: -1000 to +1000 ppm, 1 ppm steps (min. 1 Hz steps)
Clock Output	Output Level: Min 0.632 Vp-p, Max. 2 Vp-p (AC), SSB Phase Noise: ≤-80 dBc/Hz at 10 kHz offset Intrinsic Jitter: ≤20 ps (p-p), Duty cycle: 50% ± 10% Output Impedance, Connector: 50 Ω/GND, SMA
10 MHz Buff Input	Frequency: 10 MHz ±10 ppm, Output Level: Min. 0.5 Vp-p, Max 2.0 Vp-p Waveform: square wave or sine wave, Duty: 50% ±10% Input impedance, Connector: 50 Ω/GND BNC
10 MHz Ref. Output	Output Level: 1.0 Vp-p ±30% (AC), Waveform: Square wave, Duty: 50 ±10% Input impedance, Connector: 50 Ω/GND BNC

● MU181800A Clock Distributor

Operation Frequency	0.1 to 12.5 GHz
Clock Input	Input Level: 0.4 to 2.0 Vp-p Waveform: <0.5 GHz square wave, ≥0.5 GHz square wave or sine wave Input Impedance, Connector: 50 Ω/GND, SMA
Clock Output	4 ch Single-end Output Level: Min. 0.4 Vp-p, Max. 1.0 Vp-p Duty: 50% ±10% (@ 50% Clock Input Duty) Channel Skew: ≤10 ps (12.5 GHz) Output Impedance, Connector: 50 Ω/GND, SMA

● MU181020A 12.5 Gbit/s PPG

Option		MU181020A-001 9.8 to 12.5 Gbit/s	MU181020A-002 0.1 to 12.5 Gbit/s
Operating Bit Rate		9.8 to 12.5 Gbit/s 1/2 Mode: 4.9 to 6.25 Gbit/s 1/4 Mode: 2.45 to 3.125 Gbit/s 1/8 Mode: 1.225 to 1.5625 Gbit/s	0.1 to 12.5 Gbit/s
Built-in Clock		9.8 to 12.5 GHz 1/2 Mode: 4.9 to 6.25 GHz 1/4 Mode: 2.45 to 3.125 GHz 1/8 Mode: 1.225 to 1.5625 GHz Setting Resolution: 1 kHz/1 MHz	No built-in clock source
External Clock Input		Input frequency: 9.8 to 12.5 GHz or (9.8 to 12.5 GHz)/64 Input level: Min. 0.4 Vp-p, Max. 2.0 Vp-p (–4 to +10 dBm) Square wave (<0.5 GHz), Square or sine wave (≥0.5 GHz) Duty: 50% Input Impedance, Connector: 50 Ω/AC, SMA	Input frequency: 0.1 to 12.5 GHz Input level: Min. 0.4 Vp-p, Max. 2.0 Vp-p (–4 to +10 dBm) Square wave (<0.5 GHz), Square or sine wave (≥0.5 GHz) Duty: 50% Input Impedance, Connector: 50 Ω/AC, SMA
Generation Pattern	PRBS	Steps: 2 ⁿ –1 (n = 7, 9, 10, 11, 15, 20, 23, 31) Mark ratio: 1/2, 1/4, 1/8, 0/8; 1/2, 3/4, 7/8, 8/8 supported at reverse logic AND bit shift: 1 bit, 3 bits, (Prohibited at 1/2, 1/2, 0/8, 8/8 mark ratio)	
	Zero Substitution	Pattern with continuous 0s appended to M-sequence signal + 1 bit Pattern: 2 ⁿ or 2 ⁿ – 1 (n = 7, 9, 10, 11, 15, 20, 23) 0 continuous substitution count: 1 to (pattern length – 1) bits Other: 0 at next bit after 0 substitution changed to 1	
	Data	Data length: 2 to 134,217,728 bits/ch, Steps: 1 bit	
	Alternate	Data length: 128 to 67,108,864 bits/ch (independent bits for A/B) Steps: 128 bits Loop count: 511 times A/B set independently A/B switching: Internal: Auto-switching by A/B loop times setting External: Controlled by external signal Editing: Pattern editing for A/B independently	
	Mixed Pattern	Pattern: PRBS, DATA-1 to DATA-511 Data + PRBS Length: 768 to 2 ⁿ + 134,217,728, Steps: 128 bits DATA length: 512 to 134,217,728 bits	
	Sequence Pattern	Block count: 1 to 128 Block length: 8,192 to 1,048,576 bits, Steps: 128 bits Loop count: 1 to 1,024 times, Repeat Block Transition Conditions: A pattern match, B pattern match, Manual, Loop Time complete, External trigger (rising edge) Next destination: Specified Block No. or Stop	
Error Insertion		Error event: Repeat, Single, Error rate: #E – n (# = 1 to 9, n = 2 to 12) Internal/External	
Auxiliary Input		ALTN Trigger/Sequence Trigger/Error Injection/Burst Enable (Switchable) Input frequency: ≥64 bit width Input level: H: 0 V, L: –1 V Input Impedance, Connector: 50 Ω/GND, SMA	
Auxiliary Output		1/1 Mode: 1/n clock (1, 2, 4, 8, 9..., 511) 1/2 Mode: 1/n clock (1, 2, 4, 8, 9..., 255) 1/4 Mode: 1/n clock (1, 2, 4, 8, 9..., 127) 1/8 Mode: 1/n clock (1, 2, 4, 8, 9..., 63) Pattern Sync, Burst Trigger Output level: H: 0 V, L: –1 V Output Impedance, Connector: 50 Ω/GND, SMA	1/n Clock (n = 2, 4, 8, 9, 10, 11.....510, 511) Pattern Sync Output level: H: 0 V, L: –1 V Output Impedance, Connector: 50 Ω/GND, SMA
Gating Output		Burst Output Signal at Burst, Timing Signal at Repeat 1ch Output Output level: H: 0 V, L: –1 V Output Impedance, Connector: 50 Ω/GND, SMA	

Option		No Option	MU181020A-010/110	MU181020A-011/111	MU181020A-012/112
Output Number		2 (Data/Data)			
Data Output	Amplitude	—	0.05 to 0.8 Vp-p Steps: 2 mV	0.25 to 2.5 Vp-p Steps: 2 mV	0.05 to 2.0 Vp-p Steps: 2 mV
	Offset	—	-2.0 to +3.3 Voh Steps: 1 mV	-2.0 to +3.3 Voh Steps: 1 mV	-2.0 to +3.3 Voh Steps: 1 mV
	Current Limiting	—	Sourcing 50 mA/ Sinking 80 mA	Sourcing 50 mA/ Sinking 80 mA	Sourcing 50 mA/ Sinking 80 mA
	Output Level	MU181020A-001 H: 0 V/L: -0.5 V MU181020A-002 H: 0 V/L: -1.0 V	—	—	—
	Fixed I/F	—	NECL, SCFL, NCML, PCML, LVPECL (+3.3 V), LVDS		
	Crosspoint	50% ±15%	30 to 70% Steps: 1%	30 to 70% Steps: 1%	20 to 80% Steps: 1%
	Tr/Tf	MU181020A-001 (≥5 Gbit/s) 30 ps typ. (20 to 80%) MU181020A-002 (≥5 Gbit/s) 35 ps typ. (20 to 80%)	28 ps typ.(20 to 80%) (≥5 Gbit/s)	28 ps typ. (20 to 80%) (≥5 Gbit/s)	20 ps typ.(20 to 80%) (10, 12.5 Gbit/s Amplitude 2 Vp-p)
	Total Jitter	MU181020A-001 15 ps typ. MU181020A-002 10 ps typ.	MU181020A-001 15 ps p-p typ. MU181020A-002 10 ps p-p typ.	MU181020A-001 15 ps p-p typ. MU181020A-002 10 ps p-p typ.	MU181020A-001 15 ps p-p typ. MU181020A-002 8 ps p-p typ.
	Distortion (0-peak)	—	±14% typ.	25 mV ±6% typ.	25 mV ±6% typ.
	Termination	GND/50 Ω	AC, DC At DC GND, -2 V, +1.3 V, +3.3 V, Open (LVDS)/50 Ω	AC, DC At DC GND, -2 V, +1.3 V, +3.3 V, Open (LVDS)/50 Ω	AC, DC At DC GND, -2 V, +1.3 V, 3.3 V, Open (LVDS)/50 Ω
	Output	Always ON	ON/OFF		
Connector	SMA			K	
Option		No Option	MU181020A-021/121 Differential Clock Output		
Clock Output	Output Number	1 (Clock Out)	2 (Clock/Clock)		
	Amplitude	Min. 0.25 Vp-p Max 0.9 Vp-p (AC)	0.1 to 2.0 Vp-p Steps: 2 mV		
	Duty	50% ±15%	25 to 75 Steps: 1		
	Offset	—	-2.0 to +3.3 Voh Steps: 1 mV		
	Current Limiting	—	Sourcing 50 mA/Sinking 80 mA		
	Fixed I/F	—	NECL, SCFL, NCML, PCML, LVPECL (+3.3 V), LVDS		
	Tr/Tf	30 ps typ.(20 to 80%)	24ps typ.(20 to 80%)		
	Total Jitter	MU181020A-001 2ps typ.(RMS) MU181020A-002 1ps typ.(RMS)	MU181020A-001 2ps typ.(RMS) MU181020A-002 1ps typ.(RMS)		
	Termination	GND/50 Ω	AC, DC at DC GND, -2 V, +1.3 V, +3.3 V, Open (LVDS) /50 Ω		
	Output	Always ON	ON/OFF		
	Connector	SMA	K		
MU181020-030/130 Variable Data Delay (Install in MU181020A-002)		—	Phase setting range: -1 to +1 UI, Steps: 1 mUI Unit : UI/ps		

● MU181040A 12.5 Gbit/s ED

Option		MU181040A-001	MU181040-002	
Operation Bit Rate		9.8 to 12.5 Gbit/s	0.1 to 12.5 Gbit/s	
Reception Pattern	PRBS	Steps: 2^n-1 (n = 7, 9, 10, 11, 15, 20, 23, 31) Mark ratio: 1/2, 1/4, 1/8, 0/8; 1/2, 3/4, 7/8, 8/8 supported at reverse logic AND bit shift: 1 bit, 3 bits (Prohibited at 1/2, 1/2, 0/8, 8/8 mark ratio)		
	Zero Substitution	Pattern with continuous 0s appended to M-sequence signal + 1 bit Pattern: 2^n or $2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23) 0 continuous substitution count: 1 to (pattern length - 1) bits Other: 0 at next bit after 0 substitution changed to 1		
	Data	Data length: 2 to 134,217,728 bits/ch, Steps: 1 bit		
	Mixed Pattern	Pattern: PRBS, DATA-1 to DATA-511 Data + PRBS Length: 768 to $2^{31} + 134,217,728$, Steps: 128 bits DATA length: 512 to 134,217,728 bits		
	Sequence Pattern	Block count: 1 to 128		
Detection Item		Total Error, Insertion Error, Omission Error, Transition Error, Non-Transition Error		
Display Item		Bit error rate, Bit error count, Input signal frequency		
Input Signal Synchronization		Auto Sync. ON/OFF		
Error Analysis		Input signal capture (128 Mbits), Eye Margin, Eye Diagram Q measurement, Bathtub, ISI Analysis*1		
Burst Signal Measurement		Burst Trigger: Internal/External Input		
Option Number		No Option		MU181040A-020/120*2
Clock Recovery	Bit Rate	9.8 to 12.5 Gbit/s	—	0.1 GHz 0.125 to 0.2 GHz 0.25 to 0.4 GHz 0.5 to 0.8 GHz 1 to 1.6 GHz 2 to 3.2 GHz 4.25 GHz 4.9 to 6.25 GHz 9.8 to 12.5 GHz
	Recovered Clock Output	—	—	POS/NEG reversible (without MU181040A-030/130) Amplitude: 0.55 ±0.15 Vp-p Connector: SMA
Clock Input	Operating frequency range	—	0.1 to 12.5 GHz	
	Clock Source Input waveform	—	Recovered/External (MU181040A-020/120 installed) Square wave (<0.5 GHz), Square or sine wave (≥0.5 GHz), Duty cycle 50%	
	Input number	—	1	
	Input level	—	Min. 0.25 Vp-p, Max. 2.0 Vp-p	
	Termination condition	—	GND/50 Ω, Variable/50 Ω, Differential/100 Ω NECL, PCML (+3.3 V), LVPECL (+3.3 V), GND Variable: -2.5 to +3.5 V, Steps: 10 mV	
	Connector	—	SMA	

*1: Please refer the "Selection Guide for Error Detector's Functions" on the 14 pages.

*2: We recommend adding the option of MU181040A-030/130 Variable Clock Delay to perform the tests with the best phase condition when using MU181040A-020/120 Clock Recovery.

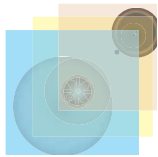
Option		MU181040A-001	MU181040A-002
Data Input	Input Number	2 (Data, $\overline{\text{Data}}$)	
	Input	Single: 50 Ω Differential: 50/100 Ω	Single: 50 Ω Differential: 50/100 Ω
	Signal Format	NRZ	
	Input Amplitude	Min. 0.1 Vp-p, Max. 0.9 Vp-p	Min. 0.1 Vp-p, Max. 2.0 Vp-p
	Threshold	-0.35 to +0.35 V, Steps: 1mV	-3.5 to +3.3 V, Steps: 1 mV
	Input Sensitivity	<50 mVp-p (12.5 Gbit/s PRBS2 ³¹ -1)	10 mVp-p typ. (12.5 Gbit/s PRBS2 ³¹ -1)
	Phase Margin	—	60 ps p-p typ. (@12.5 Gbit/s PRBS2 ³¹ -1)
	Termination Condition	AC/50 Ω	GND/50 Ω , Variable/50 Ω , Differential/100 Ω NECL, PCML (+3.3 V), LVPECL (+3.3 V), GND Variable: -2.5 to +3.5 V, Steps: 10 mV
	Connector	SMA	K
Auxiliary Input		Sequence Trigger/Capture Trigger/Burst Enable (switchable) Input frequency: ≥ 64 bit width Input level: H: 0 V, L: -1 V Input Impedance, Connector: 50 Ω /GND, SMA	
Auxiliary Output		1/16 Clock, 1/32 Clock, 1/64 Clock, Pattern Sync, Error, Sync gain Output level: H: 0 V, L: -1 V	1/N Clock (N = 8 to 511, Steps 1), Pattern Sync, Error, Sync gain Output level: H: 0 V, L: -1 V
Data Monitor Output	Output Number	—	2 (Data, $\overline{\text{Data}}$)
	Insertion Loss	—	-6 dB +1 dB/-2 dB
	Termination	—	AC/50 Ω
	Connector	—	SMA
MU181040A-030/130 Variable Clock Delay (Install in MU181040A-002)		—	Phase Setting Range: -1 UI to +1 UI Steps: 1 mUI, Unit: UI/ps

● **MU181600A Optical Transceiver (XFP)**

Electrical Input (TD)	Input waveform: NRZ, Differential Input: 0.2 to 0.8 Vp-p Input Impedance, Connector: 100 Ω differential, SMA
Electrical Output (RD)	Output waveform: NRZ, Differential Output: Min. 0.3 Vp-p, Max. 0.9 Vp-p Output Impedance, Connector: 100 Ω differential, SMA
1/1 Clock Input	Input Frequency: 9.5 to 12.5 GHz, Input Level: 0.25 to 0.8 Vp-p Input Impedance, Connector: 50 Ω /GND, SMA
1/64 Clock Output	Output Frequency: (1/1 of Clock Input) / 64, Output Level: Min. 0.32 Vp-p, Max. 0.68 Vp-p Rise/Fall Time: 300 ±100 ps (20 to 80 %), Duty: 50% ±10% Output Impedance, Connector: 50 Ω /GND, SMA
1/64 of Clock Input	Input Frequency: (Operation bitrate)/64, Input Level: 0.32 to 0.8 Vp-p Rise/Fall Time: 200 to 1250 ps (20 to 80%). Duty: 40 to 60% Input impedance, Connector: 50 Ω/GND, SMA
Optical Input/Output	Depends on mounted XFP module
XFP Insertion/Removal Times	100 times max.
Laser Safety	IEC: IEC60825-1: 2001 Class1 FDA: CDRH 21 (J) CFR 1040.10 Laser Safety Notice 50, July 2001

● **MU181601A Optical Transceiver (SFP)**

Electrical Input (TD)	Input waveform: NRZ, Single-ended Input: 0.25 to 0.6 Vp-p Input Impedance, Connector: 50 Ω Single-ended, SMA
Electrical Output (RD)	Output waveform: NRZ, Single-ended Output: Min. 0.18 Vp-p, Max. 1.0 Vp-p Output Impedance, Connector: 50 Ω Single-ended, SMA
Optical Input/Output	Depends on mounted SFP module
SFP Insertion/Removal Times	100 times max.
Laser Safety	IEC: IEC60825-1: 2001 Class1 FDA: CDRH 21 (J) CFR 1040.10 Laser Safety Notice 50, July 2001



Ordering Information

Please specify the model/order number, name and quantity when ordering.

● MP1800A

Model/Order No.	Name
MP1800A	— Main Frame — Signal Quality Analyzer
	— Standard Accessories —
	Power Cable (13 A): 1 pc
Z0306A	Wrist Strap: 1 pc
Z0541A	USB Mouse: 1 pc
B0329G	Front Cover for 3/4MW 4U: 1 pc
B0574A	MP1800A Side Protection Cover: 1 pc
MX180000A	Signal Quality Analyzer Control Software: 1 pc
Z0897A	MP1800A Operation Manual CD-ROM: 1 pc
	Windows CD-ROM: 1 pc
	— Options —
MP1800A-001*1	GPIB
MP1800A-101*2	GPIB
MP1800A-002*1	LAN
MP1800A-102*2	LAN
MP1800A-014	2 Slot for PPG and/or ED
MP1800A-015	4 Slot for PPG and/or ED
MP1800A-016	6 Slot for PPG and/or ED
	— Optional Accessories —
J0008	GPIB Cable, 2 m
Z0917A	LAN Cable (CAT5, Straight, 5 m)
Z0922A	USB Keyboard
B0588A	Rack Mount Kit
B0576A	Blank Panel
B0566A	Carrying Case
W2745AE	MP1800A Operation Manual
W2747AE	MP1800A Installation Guide
W2749AE	MX180000A Operation Manual
W2799AE	MP1800A Remote Control Manual
	— Maintenance Service —
MP1800A-ES310	Extended Three Year Warranty Service
MP1800A-ES510	Extended Five Year Warranty Service

● MT1810A

Model/Order No.	Name
MT1810A	— Main Frame — 4Slot Chassis
	— Standard Accessories —
J0491	Power Cable (13 A): 1 pc
Z0306A	Wrist Strap: 1 pc
J1109B	LAN Cable (CAT5, Straight, 5 m): 1 pc
B0575A	MT1810A Front Protection Cover: 1 pc
Z0897A	MP1800A Operation Manual CD-ROM: 1 pc
MX180000A	Signal Quality Analyzer Control Software: 1 pc
	— Options —
MT1810A-014	2 Slot for PPG and/or ED
MT1810A-015	4 Slot for PPG and/or ED
	— Optional Accessories —
B0587A	Rack Mount Kit
B0576A	Blank Panel
B0591A	Carrying Case
W2746AE	MT1810A Operation Manual
W2748AE	MT1810A Installation Guide
W2749AE	MX180000A Operation Manual
W2799AE	MP1800A Remote Control Manual
	— Maintenance Service —
MT1810A-ES310	Extended Three Year Warranty Service
MT1810A-ES510	Extended Five Year Warranty Service

● MU181000A

Model/Order No.	Name
MU181000A	— Unit /Module — 12.5 GHz Synthesizer
	— Standard Accessories —
J1349A	Coaxial Cable 0.3m: 1 pc
	— Optional Accessories —
J1137	50 Ω Terminator
J0127B	BNC Cable
W2750AE	MU181000A Operation Manual
	— Maintenance Service —
MU181000A-ES310	Extended Three Year Warranty Service
MU181000A-ES510	Extended Five Year Warranty Service

● MU181800A

Model/Order No.	Name
MU181800A	— Unit /Module — 12.5 GHz Clock Distributor
	— Optional Accessories —
J1137	50 Ω Terminator
J1349A	Coaxial Cable 0.3 m
J1343A	Coaxial Cable 1.0 m
W2751AE	MU181800A Operation Manual
	— Maintenance Service —
MU181800A-ES310	Extended Three Year Warranty Service
MU181800A-ES510	Extended Five Year Warranty Service

● MU181020A

Model/Order No.	Name
MU181020A	— Unit /Module — 12.5 Gbit/s PPG
	— Standard Accessories —
J1137	50 Ω Terminator: 3 pcs
J1341A	SMA Cover Connector: 1 pc
	— Options —
MU181020A-001	9.8 to 12.5 Gbit/s
MU181020A-002	0.1 to 12.5 Gbit/s
MU181020A-010*1	Variable Data Output (0.05 to 0.8 Vp-p)
MU181020A-110*2	Variable Data Output (0.05 to 0.8 Vp-p)
MU181020A-011*1	Variable Data Output (0.25 to 2.5 Vp-p)
MU181020A-111*2	Variable Data Output (0.25 to 2.5 Vp-p)
MU181020A-012*1	High Performance Data Output (0.05 to 2.0 Vp-p)
MU181020A-112*2	High Performance Data Output (0.05 to 2.0 Vp-p)
MU181020A-021*1	Differential Clock Output (0.1 to 2.0 Vp-p)
MU181020A-121*2	Differential Clock Output (0.1 to 2.0 Vp-p)
MU181020A-030*1	Variable Data Delay
MU181020A-130*2	Variable Data Delay
	— Standard Accessories for Option-011/111 —
J1359A	K (m)-K (f) Adapter: 2 pcs
	— Standard Accessories for Option-012/112 —
J1359A	K (m)-K (f) Adapter: 2 pcs
	— Standard Accessories for Option-021/121 —
J1359A	K (m)-K (f) Adapter: 2 pcs
J1137	50 Ω Terminator: 1 pc
	— Optional Accessories —
J1359A	K (m) - K (f) Adapter
J1137	50 Ω Terminator
J1342A	Coaxial Cable, 0.8 m
J1343A	Coaxial Cable, 1.0 m
J1360A	Measurement Kit (J1342A x 2, J1343A x 1)
W2752AE	MU181020A Operation Manual
	— Maintenance Service —
MU181020A-ES310	Extended Three Year Warranty Service
MU181020A-ES510	Extended Five Year Warranty Service

● **MU181040A**

Model/Order No.	Name
MU181040A	— Unit /Module — 12.5 Gbit/s ED
J1341A	— Standard Accessories — SMA Cover Connector: 3 pcs
	— Options —
MU181040A-001	9.8 to 12.5 Gbit/s
MU181040A-002	0.1 to 12.5 Gbit/s
MU181040A-020* ¹	Clock Recovery
MU181040A-120* ²	Clock Recovery
MU181040A-030* ¹	Variable Clock Delay
MU181040A-130* ²	Variable Clock Delay
	— Standard Accessories for Option -002 —
K1359A	K (m)-K (f) Adaptor: 2 pcs
J1137	50 Ω Terminator: 2 pcs
	— Standard Accessories for Option -020/120 —
J1137	50 Ω Terminator: 2 pcs
	— Optional Accessories —
K1359A	K (m) - K (f) Adaptor
J1137	50 Ω Terminator
J1342A	Coaxial Cable, 0.8 m
J1343A	Coaxial Cable, 1.0 m
J1360A	Measurement Kit (J1342A x 2, J1343A x 1)
W2753AE	MU181040A Operation Manual
	— Maintenance Service —
MU181040A-ES310	Extended Three Year Warranty Service
MU181040A-ES510	Extended Five Year Warranty Service

● **MU181600A**

Model/Order No.	Name
MU181600A* ³	— Unit /Module — Optical Transceiver (XFP)
	— Standard Accessories —
J1355A	Semirigid Cable: 1 pc
J0541E	Fixed Attenuator (6 dB): 2 pcs
J0541A	Fixed Attenuator (10 dB): 2 pcs
	— Optional Accessories —
J1137	50 Ω Terminator
J1342A	Coaxial Cable, 0.8 m
G0174A	850 nm XFP Module (9.95 to 11.10 Gbit/s)
G0175A	1310 nm XFP Module (9.95 to 11.30 Gbit/s)
G0176A	1550 nm XFP Module (9.95 to 10.75 Gbit/s)
J1344A	LC • PC-LC • PC-1 M-SM
J1139A	FC • PC-LC • PC-1 M-SM
J1345A	SC • PC-LC • PC-1 M-SM
J1346A	LC • PC-LC • PC-1 M-GI (62.5/125)
J1347A	FC • PC-LC • PC-1 M-GI (62.5/125)
J1348A	SC • PC-LC • PC-1 M-GI (62.5/125)
Z0282	Ferrule cleaner
Z0283	Ferrule cleaning tape (6 pcs/set)
Z0284	Adapter cleaner (Stick type, 200 pcs/set)
W2754AE	MU181600A/MU181601A Operation Manual
	— Maintenance Service —
MU181600A-ES310	Extended Three Year Warranty Service
MU181600A-ES510	Extended Five Year Warranty Service

● **MU181601A**

Model/Order No.	Name
MU181601A* ⁴	— Unit /Module — Optical Transceiver (SFP)
	— Standard Accessories —
J0541E	Fixed Attenuator (6 dB): 1 pc
	— Optional Accessories —
J1137	50 Ω Terminator
J1343A	Coaxial Cable, 1.0 m
G0177A	850 nm SFP Module (1.062 to 4.25 Gbit/s)
G0178A	1310 nm SFP Module (0.155 to 2.67 Gbit/s)
G0179A	1550 nm SFP Module (0.155 to 2.67 Gbit/s)
J1344A	LC • PC-LC • PC-1 M-SM
J1139A	FC • PC-LC • PC-1 M-SM
J1345A	SC • PC-LC • PC-1 M-SM
J1346A	LC • PC-LC • PC-1 M-GI (62.5/125)
J1347A	FC • PC-LC • PC-1 M-GI (62.5/125)
J1348A	SC • PC-LC • PC-1 M-GI (62.5/125)
Z0282	Ferrule cleaner
Z0283	Ferrule cleaning tape (6 pcs/set)
Z0284	Adapter cleaner (Stick type, 200 pcs/set)
W2754AE	MU181600A/MU181601A Operation Manual
	— Maintenance Service —
MU181601A-ES310	Extended Three Year Warranty Service
MU181601A-ES510	Extended Five Year Warranty Service

● **Software**

Model/Order No.	Name
MX180001A	SONET/SDH Pattern Editor
W2884AE	MX180001A Operation Manual
MX180003A	GbE/10 GbE Pattern Editor
W2886AE	MX180003A Operation Manual
MX180004A	PON Application Software
W2887AE	MX180004A Operation Manual

*1: Original order option

*2: Upgrade option to original order

*3: The XFP module is sold separately. Note that Anritsu supports only XFP modules purchased from Anritsu.

*4: The SFP module is sold separately. Note that Anritsu supports only SFP modules purchased from Anritsu.

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