Specifications

This chapter provides a general description of the logic analyzer module and a list of specifications under Characteristic Tables beginning on page 1–2.

Product Description

The logic analyzer module is designed to be used with either the benchtop mainframe or portable mainframe in a TLA 700 Series Logic Analyzer. The logic analyzer module is used as a test and measurement tool for high-speed digital timing and state acquisition across several channels.

Some of the key features of the logic analyzer module include the following:

- Standard channel widths and memory depths as listed in Table 1–1

Table 1–1: Logic analyzer module variations

Product	Number of channels	Memory depth
TLA 7L1	34	32 K[1]
TLA 7L2	68	32 K[1]
TLA 7L3	102	32 K[1]
TLA 7L4	136	32 K[1]
TLA 7M1	34	512 K
TLA 7M2	68	512 K
TLA 7M3	102	512 K
TLA 7M4	136	512 K

[1] **PowerFlex configurable to 128 K**

- 100 MHz synchronous acquisition with a programmable setup and hold window (PowerFlex configurable to 200 MHz)
- 250 MHz asynchronous full depth selections with selectable sampling rates
- 2 GHz asynchronous acquisition into a 2 K high resolution timing buffer
- 250 MHz trigger capability, plus special setup and hold violation triggering and glitch triggering
- Data correlation with other modules

Characteristic Tables

This section lists the specifications for the logic analyzer module. All specifications are guaranteed unless noted *Typical*. Specifications that are marked with the ✓ symbol are checked directly (or indirectly) in the *TLA 700 Series Performance Verification and Adjustment Technical Reference Manual*. The specifications apply to all versions of the logic analyzer module unless otherwise noted.

The performance limits in this specification are valid with these conditions:

- The logic analyzer module must have been calibrated/adjusted at an ambient temperature between +20° C and +30° C.
- The logic analyzer module must be in an environment with temperature, altitude, humidity, and vibration within the operating limits described in these specifications.
- The logic analyzer module must have had a warm-up period of at least 30 minutes.
- The logic analyzer module must have had its signal-path-compensation routine (self calibration) last executed after at least a 30 minute warm-up period.

Table 1–2: Channel width and depth

Characteristic	Description	
Number of channels	Product	Channels
	TLA 7L1 and TLA 7M1	32 data and 2 clock
	TLA 7L2 and TLA 7M2	64 data and 4 clock
	TLA 7L3 and TLA 7M3	96 data, 4 clock, and 2 qualifier
	TLA 7L4 and TLA 7M4	128 data, 4 clock, and 4 qualifier
Acquisition memory depth	Product	Memory depth
	TLA 7L1, TLA 7L2, TLA 7L3, TLA 7L4	32 K[1]
	TLA 7M1, TLA 7M2 ,TLA 7M3, TLA 7M4	512 K

1 **PowerFlex configurable to 128 K**

Table 1–3: Clocking

Characteristic	Description	
Asynchronous clocking		
✓ Internal sampling period[1]	4 ns to 50 ms in a 1–2–5 sequence	
✓ Minimum recognizable word[2] (across all channels)	Channel-to-channel skew + sample uncertainty Example: for a P6417 Probe and a 4 ns sample period = 1.6 ns + 4 ns = 5.6 ns	
Synchronous clocking		
Number of clock channels[3]	Product	Clock channels
	TLA 7L1 and TLA 7M1	2
	TLA 7L2 and TLA 7M2	4
	TLA 7L3 and TLA 7M3	4
	TLA 7L4 and TLA 7M4	4
Number of qualifier channels	Product	Qualifier channels
	TLA 7L1 and TLA 7M1	0
	TLA 7L2 and TLA 7M2	0
	TLA 7L3 and TLA 7M3	2
	TLA 7L4 and TLA 7M4	4
✓ Setup and hold window size (data and qualifiers)	Maximum window size = Maximum channel-to-channel skew + (2 x sample uncertainty) + 0.4 ns Maximum setup time = User interface setup time + 0.6 ns Maximum hold time = User interface hold time + 0.4 ns Maximum setup time for slave module of merged pair = User Interface setup time + 0.8 ns Maximum hold time for slave module of merged pair = User Interface hold time + 0.7 ns Example: for P6417 Probe and user interface setup & hold of 2.0/0.0 typical Maximum setup time = 2.0 ns + 0.6 ns = 2.6 ns Maximum hold time = 0.0 ns + 0.4 ns = 0.4 ns	
Setup and hold window size (data and qualifiers) (*Typical*)	Channel-to-channel skew (*typical*) + (2 x sample uncertainty) Example: for P6417 Probe = 1 ns + (2 x 500 ps) = 2 ns	
Setup and hold window range	The setup and hold window can be moved for each channel group from +8.5 ns (Ts) to –7.0 ns (Ts) in 0.5 ns steps (setup time). Hold time follows the setup time by the setup and hold window size.	
✓ Maximum synchronous clock rate[4]	200 MHz in full speed mode (5 ns minimum between active clock edges) 100 MHz in half speed mode (10 ns minimum between active clock edges)	

Table 1–3: Clocking (Cont.)

Characteristic	Description
Demux clocking	
Demux Channels (TLA 7L3 ,TLA 7L4, TLA 7M3, TLA 7M4)	Channels multiplex as follows: A3(7:0) to D3(7:0) A2(7:0) to D2(7:0) A1(7:0) to D1(7:0) A0(7:0) to D0(7:0)
(TLA 7L1, TLA 7L2, TLA 7M1, TLA 7M2)	Channels multiplex as follows: A3(7:0) to C3(7:0) A2(7:0) to C2(7:0) A1(7:0) to D1(7:0) TLA 7L2 and TLA 7M2 only A0(7:0) to D0(7:0) TLA 7L2 and TLA 7M2 only
Time between DeMux clock edges[4] (*Typical)*	5 ns minimum between DeMux clock edges in full-speed mode 10 ns minimum between DeMux clock edges in half-speed mode
Time between DeMux store clock edges[4] (*Typical)*	10 ns minimum between DeMux master clock edges in full-speed mode 20 ns minimum between DeMux master clock edges in half-speed mode
Clocking state machine	
Pipeline delays	Each channel can be programmed with a pipeline delay of 0 through 3 active clock edges.

1 It is possible to use storage control and only store data when it has changed (transitional storage).

2 Applies to asynchronous clocking only. Setup and hold window specification applies to synchronous clocking only.

3 Any or all of the clock channels may be enabled. For an enabled clock channel, either the rising, falling, or both edges can be selected as the active clock edges. The clock channels are stored.

4 Full and half speed modes are controlled by PowerFlex options and upgrade kits.

Table 1–4: Trigger system

Characteristic	Description
Triggering Resources	
Word/Range recognizers	16 word recognizers. The word recognizers can be combined to form full width, double bounded, range recognizers. The following selections are available: 16 word recognizers — 0 range recognizers 13 word recognizers — 1 range recognizer 10 word recognizers — 2 range recognizers 7 word recognizers — 3 range recognizers 4 word recognizers — 4 range recognizers
Range recognizer channel order	From most-significant probe group to least-significant probe group: C3 C2 C1 C0 E3 E2 E1 E0 A3 A2 D3 D2 A1 A0 D1 D0 Q3 Q2 Q1 Q0 CK3 CK2 CK1 CK0 Missing channels for modules with fewer than 136 channels are omitted. When merged, the range recognition extends across the two modules; the master module contains the most-significant groups.
Glitch detector[1,2]	Each channel group can be enabled to detect a glitch
Minimum detectable glitch pulse width (*Typical)*	2.0 ns (single channel with P6417 probe)
Setup and hold violation detector[1,3]	Each channel group can be enabled to detect a setup and hold violation. The range is from 8 ns before the clock edge to 8 ns after the clock edge. The range can be selected in 0.5 ns increments. The setup and hold violation of each window can be individually programmed.
Transition detector[1, 4]	Each channel group can be enabled or disabled to detect a transition between the current valid data sample and the previous valid data sample.
Counter/Timers[5,6]	2 counter/timers, 51 bits wide, can be clocked up to 250 MHz. Maximum count is 2^{51} Maximum time is 9.007^{6} seconds or 104 days
Signal In 1	A backplane input signal
Signal In 2	A backplane input signal
Trigger In	A backplane input signal that causes the main acquisition and the MagniVu acquisition to trigger if they are not already triggered.
Active trigger resources[7]	16 maximum (excluding counter/timers)
Trigger States	16
✓ Trigger State sequence rate	Same rate as valid data samples received, 250 MHz maximum
Trigger Machine Actions	
Main acquisition trigger	Triggers the main acquisition memory
Main trigger position	Trigger position is programmable to any data sample (4 ns boundaries)
Increment counter	Either of the two counter/timers used as counters can be incremented.
Start/Stop timer	Either of the two counter/timers used as timers can be started or stopped.

Table 1–4: Trigger system (Cont.)

Characteristic	Description
Reset counter/timer	Either of the two counter/timers can be reset. When a counter/timer used as a timer and is reset, the timer continues in the started or stopped state that it was in prior to the reset.
Signal out	A signal sent to the backplane to be used by other modules
Trigger out	A trigger out signal sent to the backplane to trigger other modules
Storage Control	
Global storage	Storage is allowed only when a specific condition is met. This condition can use any of the trigger machine resources except for the counter/timers. Storage commands defined in the current trigger state will override the global storage control. Global storage can be used to start the acquisition with storage initially turned on (default) or turned off.
By event	Storage can be turned on or off; only the current sample can be stored. The event storage control overrides any global storage commands.
Block storage[8]	When enabled, 31 samples are stored before and after the valid sample.
Glitch violation storage	The acquisition memory can be enabled to store glitch violation information with each data sample when asynchronous clocking is used. The probe data storage size is reduced by one half (the other half holds the violation information). The fastest asynchronous clocking rate is reduced to 10 ns.

1 Each use of a glitch detector, setup and hold violation detector, or transition detector requires a trade-off of one word recognizer resource.

2 Any glitch is subject to pulse width variation of up to the channel-to-channel skew specification + 0.5 ns.

3 Any setup value is subject to variation of up to 1.6 ns; any hold value is subject to variation of up to 1.4 ns.

4 This mode can be used to create transitional storage selections where all channels are enabled.

5 Counters can be used as setable, resetable, or testable flags and have zero reset latency.

6 Timers can be used as testable flags with TLA 7Lx and TLA 7Mx Modules with serial numbers B020000 and higher and TLA 700 Series Software Version 1.10 or higher.

7 Word recognizers are traded off one-by-one as Signal In 1, Signal In 2, glitch detection, setup and hold detection, or transition detection resources are added.

8 Block storage is disallowed when glitch storage or setup and hold violation is enabled.

Table 1–5: Input parameters (with P6417 Probe)

Characteristic	Description
✓ Threshold Accuracy	±100 mV
Threshold range and step size	Setable from +5 V to –2 V in 50 mV steps
Threshold channel selection	16 threshold groups assigned to channels. Each probe has two threshold settings, one for the clock/qualifier channel and one for the data channels.
✓ Channel-to-channel skew	≤ 1.6 ns maximum (When merged, add 0.5 ns for the slave module.)
Channel-to-channel skew (*Typical)*	≤ 1.0 ns typical (When merged, add 0.3 ns for the slave module.)
Sample uncertainty	
Asynchronous:	Sample period
Synchronous:	500 ps
Probe input resistance (*Typical*)	20 kΩ
Probe input capacitance (*Typical*)	2 pF maximum
Minimum slew rate (*Typical*)	0.2 V/ns
Maximum operating signal	6.5 V_{p-p} –3.5 V absolute input voltage minimum 6.5 V absolute input voltage maximum
Probe overdrive	±250 mV or ±25% of signal swing minimum required beyond threshold, whichever is greater ±4 V maximum beyond threshold
Maximum nondestructive input signal to probe	±15 V
Minimum input pulse width signal (single channel) (*Typical*)	2 ns
Delay time from probe tip to input probe connector (*Typical*)	7.33 ns

Table 1–6: MagniVu feature

Characteristic	Description
MagniVu memory depth	2016 samples per channel
MagniVu sampling period	Data is asynchronously sampled and stored every 500 ps in a separate high resolution memory; there are no clocking options.

Table 1–7: Merged modules

Characteristic	Description
Number of modules that can be merged together	Two adjacent modules regardless of channel widths and memory depths (TLA 7L3, TLA 7L4, TLA 7M3, TLA 7M4 only)
Number channels after merge	The sum of the data channels of both modules plus the CLK/QUAL channels (active clocks for the merge system) of the master module plus the CLK/QUAL channels (nonactive stored clock channels to the merge system)
Merge system acquisition depth	Channel depth is equal to the smaller depth of the two modules.
Number of clock and qualifier channels after merge	Same number of clock and qualifier channels on the master module. The clock and qualifier channels on the slave module have no effect on clocking and are only stored.
Merge system triggering resources	Triggering resources are the same as a single module except that the widths of the word/range recognizers, setup and hold violation detector, glitch detector, and transition detector are increased to the merged channel width.

Table 1–8: Data handling

Characteristic	Description
Nonvolatile memory retention time (*Typical*)	Battery is integral to the NVRAM. Battery life is > 10 years.

Table 1–9: Atmospherics

Characteristic	Description
Altitude	
Operating	To 15,000 ft. (4570 m) provided maximum ambient temperature is derated by 1° C/1000 ft. above 1000 ft.
Nonoperating	40,000 ft. (12190 m)
Temperature	
Operating	0° C to 50° C (32° F to +122° F) for exterior air when operated in an appropriate mainframe. Maximum operating temperature is derated by 1° C/1000 ft. above 1000 ft.
Nonoperating	–40° to +71° C (–40° F to +160° F)
Humidity	
Operating and nonoperating	To 95% relative humidity at or below 30° C (86° F) To 45% relative humidity up to 50° C (122° F)

Table 1–10: Mechanical

Characteristic	Description
Construction material	
Chassis parts	Aluminum alloy
Front panel	Plastic laminate
Circuit boards	Glass laminate
Cabinet	Aluminum
Weight	5 lbs 10 oz. (2.55 kg) for TLA 7L4 or TLA 7M4 8 lbs (3.63 kg) for TLA 7L4 or TLA 7M4 packaged for domestic shipping
Overall dimensions	
Height	10.32 in. (26.2 cm.)
Width	2.39 in. (6.1 cm.)
Depth	14.7 in. (37.3 cm.)
Probe cables	
P6417 length	6 ft. (1.8 m.)
Mainframe interlock	1.4 ECL keying is implemented

Table 1–11: Certifications and compliances

EC Declaration of Conformity – EMC	Meets intent of Directive 89/336/EEC for Electromagnetic Compatibility. Compliance was demonstrated to the following specifications as listed in the Official Journal of the European Communities:	
	EN 55011	Class A Radiated and Conducted Emissions
	EN 50081-1 Emissions:	
	EN 60555-2	AC Power Line Harmonic Emissions
	EN 50082-1 Immunity:	
	IEC 801-2	Electrostatic Discharge Immunity
	IEC 801-3	RF Electromagnetic Field Immunity
	IEC 801-4	Electrical Fast Transient/Burst Immunity
	IEC 801-5	Power Line Surge Immunity