Logic Analyzer Description

The HP 16517A/18A Synchronous Timing Analyzer module is part of a family of general-purpose logic analyzers. The HP 16517A/18A is a multi-card module that is used with the HP 16500 mainframes and the HP 16501A Expansion Frame.

The HP 16500 mainframe is designed for use by digital and microprocessor hardware and software designers. The HP 16500 mainframe has HP-IB, RS-232-C, and Ethernet LAN interfaces for hard copy printouts, postprocessing of measurement data, and control by a host computer.

The HP 16517A/18A analyzer can be configured in the following ways:

- The HP 16517A master can run as a single-card module or have up to four HP 16518A expansion cards added for a multi-card module.
- Channel width varies from 16 channels on the HP 16517A master, up to 80 channels when four HP 16518A expansion cards are added.
- Channel memory depth is 64 Kbytes in both full-channel state and timing modes or 128 Kbytes in half-channel timing mode.

Timing Modes

The HP 16517A/18A has two timing modes. In full-channel timing mode, data is sampled at up to 2 GHz. In half-channel timing mode, data is sampled at 4 GHz.

Synchronous State Mode

In the full-channel state mode, a synchronous external clock running at speeds up to 1 GHz can be used as the sample clock. In addition, the sample point can be offset to ensure a sample where you know data is valid.

Not only can you sample at the external clock transitions, but you can set the analyzer to oversample, in powers of two, up to 32x, or, up to a maximum of 2 GHz sample rate. Each point of oversampling is precisely distributed evenly within the external clock period.

Triggering

Defining a trigger specification is as easy as picking a predefined macro from a trigger macro library. Trigger macros can be used by themselves or in combination with each other. Resource terms include four global patterns, two global edges, and one level dependent timer/counter. By using trigger macros, or defining your own trigger specification, the user-friendly and flexible triggering architecture lets you create a large array of trigger sequencing or qualification needed.

Acquisition Control

Data storage can begin at either the start, center, end, or a user-defined point within memory. In addition, if the data of interest occurs a relatively long time after trigger, you can delay storage after a trigger by a user-defined amount. With all the acquisition control available, you can fill acquisition memory very efficiently.

Measurement Display

Measurement data is displayed as waveforms or state data listings. State data can be compared bit by bit to a user-defined reference image. In the state listing, you can choose to display either sample clock transitions or both sample clock and oversampling clock transitions. In the timing waveform display, you can show state values integrated in the waveform.

User Interface

The HP 16500 Logic Analysis System has four easy-to-use user interface devices: the knob, the touchscreen, the optional mouse (standard in the HP 16500C), and the optional keyboard.

The knob on the front panel is used to move the cursor on certain menus, to increment or decrement numeric fields, and to roll the display.

The touchscreen fields can be selected by touch or with the optional mouse. To activate a touchscreen field by touch, simply touch the screen over any dark blue box on the display with your finger until the field changes color. Then remove your finger from the screen to activate your selection. The area under your finger when you remove it from the screen is the area selected.

To activate a field with the mouse, position the cursor (+) of the mouse over the desired field and press the left button of the mouse.

The keyboard can control all instrument functions by using special function keys, the arrow keys, and the ENTER key. Alphanumeric entry is simply typed in.

All user interface devices are discussed in more detail in the HP 16500 User's Reference.

Configuration Capabilities

The logic analyzer can be configured as a single- or multi-card module. The number of data channels range from 16 channels using just the HP 16517A, up to 80 channels when four HP 16518A expansion cards are connected. A half-channel acquisition mode is available which reduces the channel width by half, but doubles memory depth from 64 Kbits to 128 Kbits per channel. The configuration guide below illustrates the channel width and memory depth combinations in all acquisition modes.

Table 1-1

Conventional Timing Modes

	One-Card Module	Two-Card Module	Three-Card Module	Four-Card Module	Five-Card Module
Full Channel	16 channels 64 Kbits Deep	32 channels 64 Kbits Deep	48 channels 64 Kbits Deep	64 channels 64 Kbits Deep	80 channels 64 Kbits Deep
Half Channel	8 channels 128 Kbits Deep	16 channels 128 Kbits Deep	24 channels 128 Kbits Deep	32 channels 128 Kbits Deep	40 channels 128 Kbits Deep

Table 1-2

Synchronous State Mode

	One-Card Module	Two-Card Module	Three-Card Module	Four-Card Module	Five-Card Module
Full Channel	16 channel 64 Kbits Deep	32 channel 64 Kbits Deep	48 channel 64 Kbits Deep	64 channel 64 Kbits Deep	80 channel 64 Kbits Deep

Accessories Supplied

The table below lists the accessories supplied with your logic analyzer. If any of these accessories are missing, contact your nearest Hewlett-Packard sales office. If you need additional accessories, refer to *Accessories for HP Logic Analyzers* .

Table 1-3 Accessories Supplied

Accessory	Quantity
Probe Pod	2
Probe Accessory Kit	1
Cable Assembly	1
Operating system disks	1
User's Reference	1

Accessories Available

There are a number of accessories available that will make your measurement tasks easier and more accurate. You will find these listed in *Accessories for HP Logic Analyzers*, available from your HP Sales Office.

Specifications

The specifications are the performance standards against which the product is tested. They are specified for an input signal VH = –0.9V, VL = –1.7V, slew rate = 1V/ns, and threshold = –1.3V.

Minimum Input Voltage Swing: 500 mV peak to peak.

Threshold Accuracy: ± 2% of input signal ± 50 mV.

Minimum External Clock Period: 1 ns.

Setup/Hold:

Per pod*	350 ps/350 ps.
Across pods	750 ps/750 ps.
	350 ps/350 ps, with manual deskew.

Actual setup/hold adjustable with sample offset in all modes.

* For the frequency range of 62.5 MHz to 20 MHz, a duty cycle of 40% to 60% is required.

Characteristics

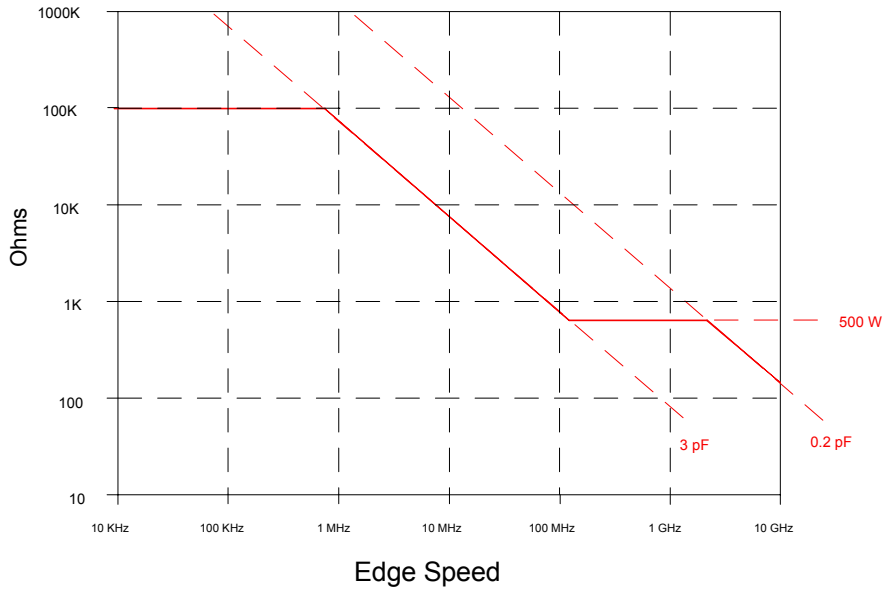
The characteristics are not specifications, but are included as additional information.

Probes

Input DC Resistance: 100 KΩ, ± 2%.

Input Impedance:

DC through 400 ns rise time	100 KΩ, typical.
3.5 ns through 350 ps	500 Ω, typical.



Impedance Plot

Probes

Input Capacitance: 0.2 pF and then, through 500 Ω, 3 pF.

Minimum Input Overdrive: 250 mV or 30% of input (whichever is greater) above the pod threshold.

Threshold Range Increments: ±5.0 V in 10 mV increments.

Threshold Setting: Preset TTL, ECL, or User-defined on a per pod basis.

Input Dynamic Range: ±5 V about the threshold.

Maximum Input Voltage: 40 V peak-to-peak, CAT 1.

Synchronous State Analysis

Maximum External Clock Speed: 1 GHz, requires a periodic clock.

Minimum State Speed: 20 MGSa/s, requires a periodic clock.

Minimum Detectable Pulse Width: 900 ps.

Channel Count: 16 per card, up to 80 in one frame.

Channel-to-Channel Skew across up to 80 channels:

Per pod	250 ps, typical.
Across pods	1 ns, typical.
	250 ps, with manual deskew.

Memory Depth per Channel: 65536 samples.

State Clocks: One external clock is available on the master board. No clocks are available on the expander board. Clock edge is selectable as positive or negative.

State Clock Duty Cycle Range:

1 GHz through 500 MHz	45% - 55%, typical.
500 MHz through 250 MHz	30% - 70%, typical.
250 MHz through 20 MHz	20% - 80%, typical.

Oversampling: 2x, 4x, 8x, 16x, and 32x, with a maximum rate of 2 GSa/s.

Timing Analysis

Timing Modes: Conventional timing.

Timing Speed: 15.3 KSa/s – 2 GSa/s full channel, 4 GSa/s half channel.

Sample Period: 500/250 ps minimum (full/half channel mode), 65.536 µs maximum.

Channel Count: 16/8 per card (full/half channel mode).

Minimum Detectable Pulse Width:

4 GSa/s	800 ps, typical.
2 GSa/s or less	1.1 ns, typical.

Memory Depth per Channel: 65536 samples full channel mode; 131072 samples, half channel mode.

Time Covered by Data: 32.8 µs at 2 GSa/s or 4 GSa/s up to 4.3 s at 15.3 KSa/s.

Time Interval Accuracy: ± (sample period + channel-to-channel skew + 0.005% of time interval reading).

Sample Period Accuracy: 0.005% of sample period.

Channel-to-Channel Skew across up to 80 channels: 250 ps, typical.

Maximum Delay After Triggering: (2 to the 20th)×(sample period), or 16.78 ms at or below 16 ns sample period.

Note: When oversampling, use oversampled period for sample period above.

Trigger Characteristics

Pattern Recognizers: 4. Each pattern recognizer is the AND combination of bit (0, 1, or X) patterns.

Pattern Width: 16/32/48/64/80 channels.

Minimum Pattern Recognizer Pulse Width: 2.25 ns.

Edge Recognizers (Timing only): 2. Trigger on a rising, falling, or either edge on any channel. Edges are OR'd across all channels.

Edge Width: 16/32/48/64/80 channels.

Edge Counting Frequency: 444 MHz.

Edge Detection: Up to 1 GHz.

Greater than Duration (Timing only): 0 ns – 510 ns, accuracy is ± 2.25 ns.

Less than Duration (Timing only): 4 ns – 510 ns, accuracy is ± 2.25 ns.

Qualifier: A user-specified term that can be any state, no state, any recognizer (patterns or edges), the timer, or the logical combination (AND, OR, XOR) of the recognizers and timers.

Branching: Each sequence level has two branching qualifiers. When satisfied, the analyzer will branch to the specified sequence level.

Maximum Occurrence Count: 16,777,216.

Maximum Sequencer Speed: 500 MHz.

State Sequence Levels: 4 plus trace point.

Timing Sequence Levels: 4 plus trace point.

Timer/Counter: There is one timer or counter per sequence level, which is restarted upon entry into each level.

Timer/Counter Range:

Timing mode	0 s to 33 ms.
State mode	500 MHz to 1 GHz, (user clock period)×(2 to the 23rd). below 500 MHz, (user clock period)×(2 to the 24th).

Timer Resolution:

Timing mode	2 ns.
State mode	above 500 MHz, 2 × user clock period. below 500 MHz, user clock period.

Timer Accuracy: 0.005% of timer value.

Measurement and Display Functions

Arming: Can be armed by the Run key, the external SMB, or the Intermodule Bus (IMB).

Trace Mode: Single mode acquires data once per trace specification. Repetitive mode repeats single mode acquisitions until Stop is pressed or until pattern time interval or compare stop criteria are met.

Labels: Channels may be grouped together and given a 6-character name. Up to 126 labels may be assigned with up to 32 channels per label in each analyzer. Trigger terms may be given an 8-character name.

Activity Indicators: Provided in the Format menu for monitoring device-under-test activity while setting up the analyzer. The indicators only function when the analyzer is stopped.

Pod ID: A button provided on each pod which, when pressed, causes the display of its slot letter and pod number on the analyzer screen.

Markers: Two markers (X and O) are shown as dashed lines in the display.

Trigger: Displayed as a red vertical dashed line in the waveform and chart display and as line 0 in the listing and compare displays.

Measurement Functions

Run: Starts acquisition of data in specified trace mode.

Stop: In single trace mode or the first run of a repetitive acquisition, Stop halts acquisition and displays the current acquisition data. For subsequent runs in repetitive mode, Stop halts acquisition of data and does not change current display.

Time Interval: The X and O markers measure the time interval between events.

Patterns: The X or O marker can be used to locate the nth occurrence of a specified pattern before or after trigger, or after the beginning of data. The O marker can also find the nth occurrence of a pattern before or after the X marker.

Statistics: X to O marker statistics are calculated for repetitive acquisitions. Patterns must be specified for both markers, and statistics are kept only when both patterns can be found in an acquisition. Statistics are minimum X to O time, maximum X to O time, average X to O time, and ratio of valid runs to total runs.

Compare Mode Functions: Performs a post-processing bit-by-bit comparison of the acquired state data and Compare Reference data.

Compare Reference: Created by copying an acquisition into the compare reference buffer. Allows editing of any bit in the Compare Reference to a 1, 0 or X.

Compare Reference Boundaries: Each channel (column) in the compare reference can be enabled or disabled via bit masks. Upper and lower ranges of states (rows) in the compare reference can be specified. Any data bits that do not fall within the enabled channels and the specified range are not compared.

Stop Measurement: Repetitive acquisitions may be halted when the comparison between the current acquisition and the Compare Image is equal or not equal.

Compare Mode Display: Reference Listing display shows the Compare Reference and bit masks. Difference Listing display highlights differences between the current acquisition and the Compare Reference.

Data Entry/Display

Display Modes: Listing, Waveform, Chart, Compare Reference Listing, and Compare Difference Listing. Time-correlated oscilloscope traces can also be displayed in the waveform display mode when the intermodule bus is used.

Markers: Correlated to listing, chart, and waveform displays. Available as pattern, time, or statistics.

Waveform Displays: Display acquisition in waveform format.

Sec/div: 250 ps to 50 s.

Delay: –2,500 s to +2,500 s.

Accumulate: Waveform display is not erased between successive acquisitions.

Overlay Mode: Multiple channels can be displayed on one waveform display line. When waveform size is set to large, the value represented by the waveforms is displayed inside the waveforms in selected base.

Displayed Waveforms: 24 lines maximum on one screen. Up to 96 lines may be specified and scrolled through.

Bases: Binary, octal, decimal, hexadecimal, ASCII (data displays only), user-defined symbols, and two's complement.

Pattern Symbols: User can define a mnemonic for the specific bit pattern of a label. When label base is SYMBOL, mnemonic is displayed where the bit pattern occurs.

Range Symbols: User can define a mnemonic covering a range of values. When data display is SYMBOL, values within the specified range are displayed as mnemonic + offset from base of range.

Number of Symbols: 1000 maximum.

Operating Environment

Temperature	Instrument, 0 °C to 55 °C (+32 °F to 131 °F). Probe lead sets and cables, 0 °C to 65 °C (+32 °F to 149 °F).
Humidity	Instrument, probe lead sets, and cables, up to 95% relative humidity at +40 °C (+122 °F).
Altitude	To 4600 m (15,000 ft).
Vibration	Operating: Random vibration 5 to 500 Hz, 10 minutes per axis, ≈ 0.3 g (rms). Non-operating: Random vibration 5 to 500 Hz, 10 minutes per axis, ≈ 2.41 g (rms); and swept sine resonant search, 5 to 500 Hz, 0.75 g (0-peak), 5 minute resonant dwell at 4 resonances per axis.